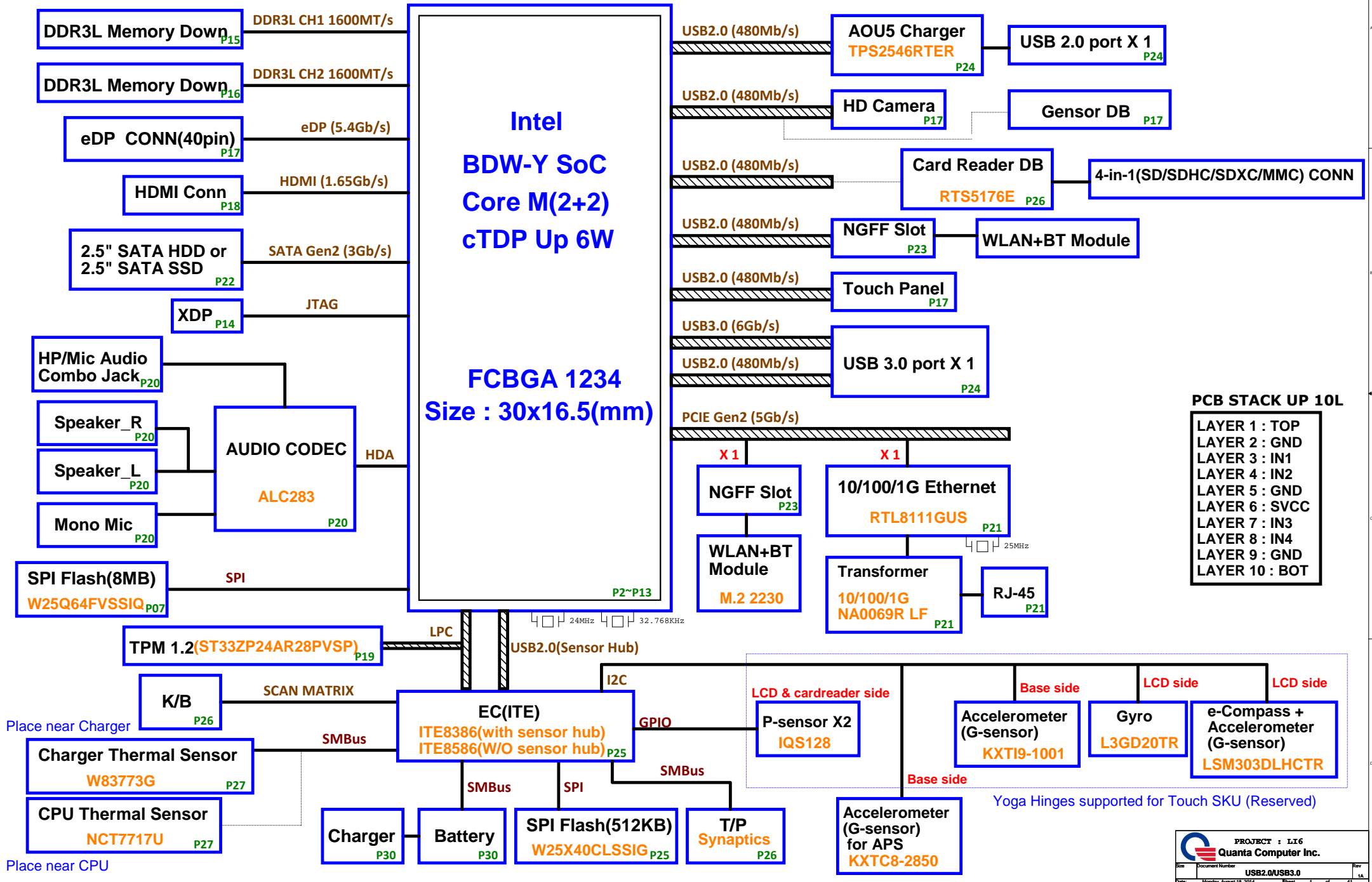
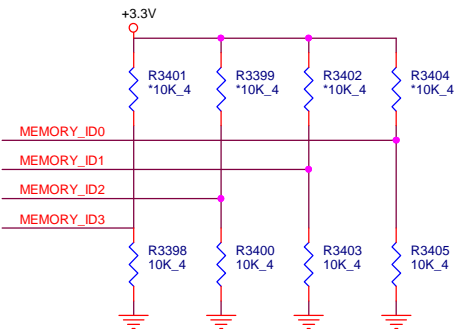
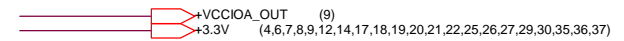
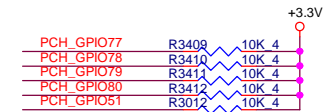
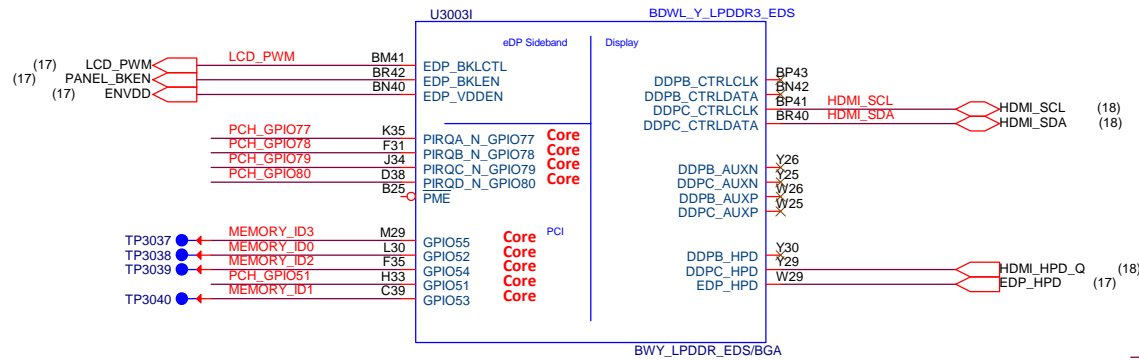
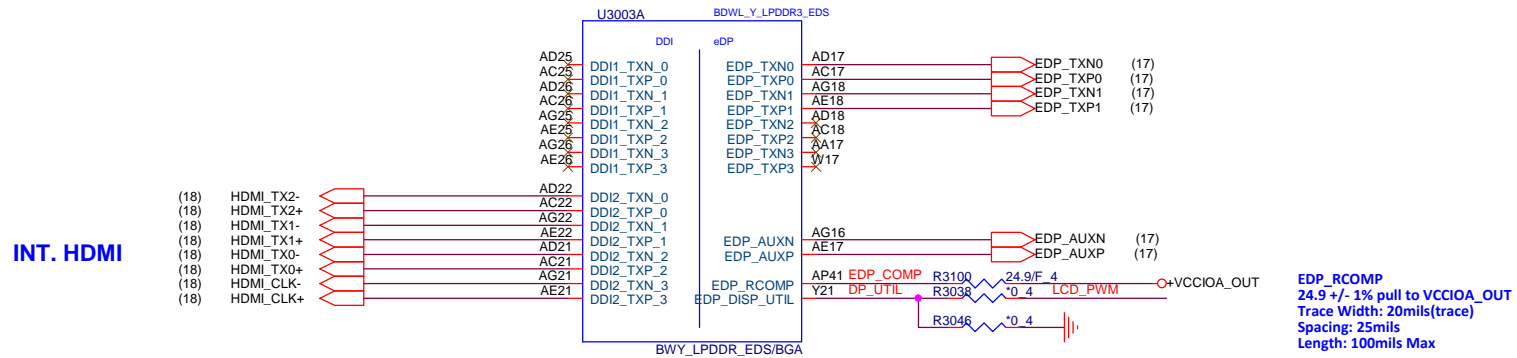


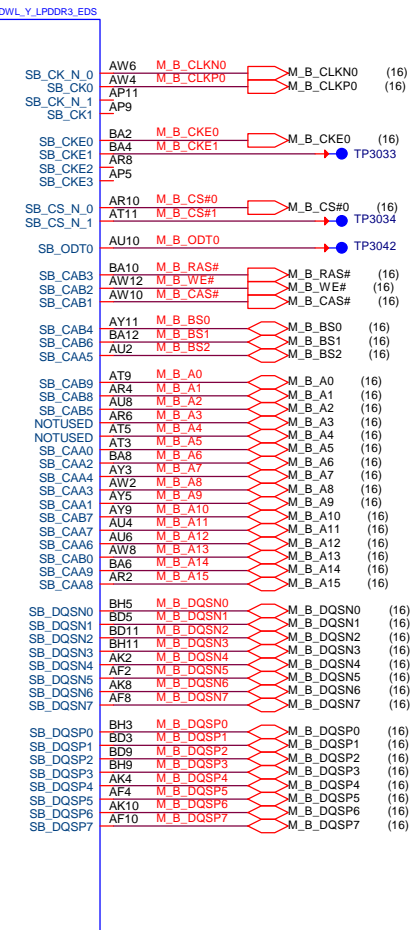
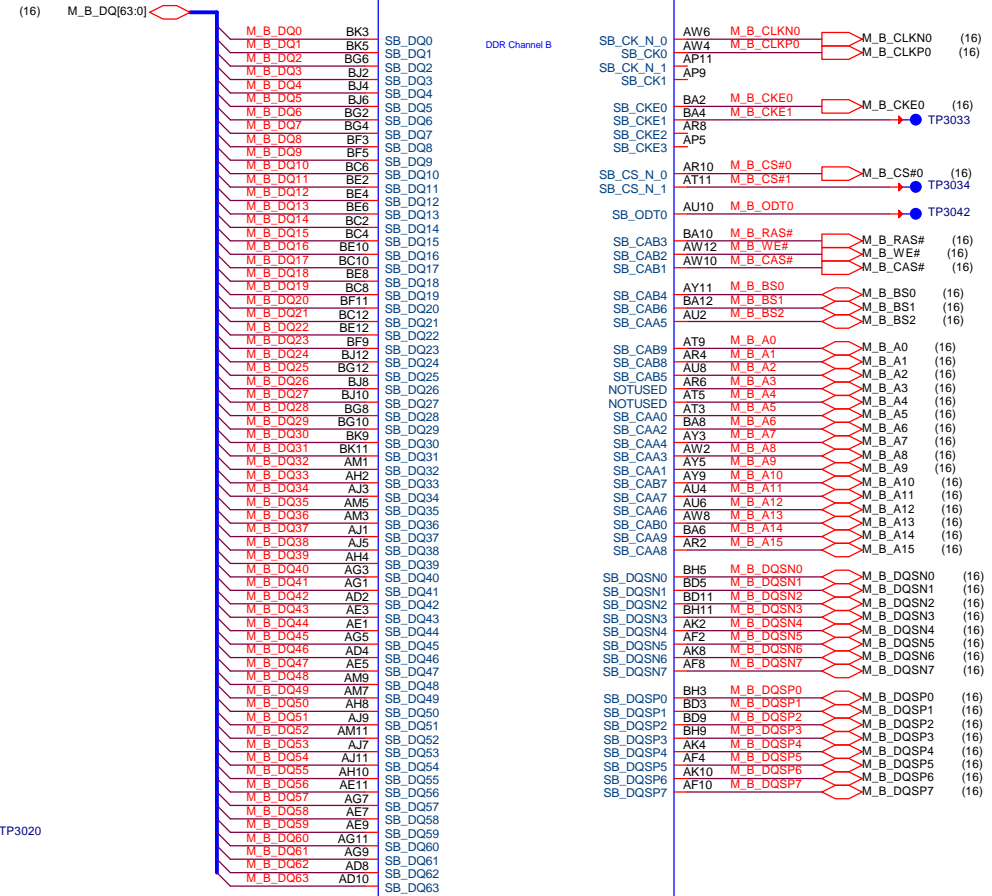
# MR1.5 Intel BDW-Y Platform UMA Block Diagram (Windows)



## Broadwell Type-Y (DISPLAY)



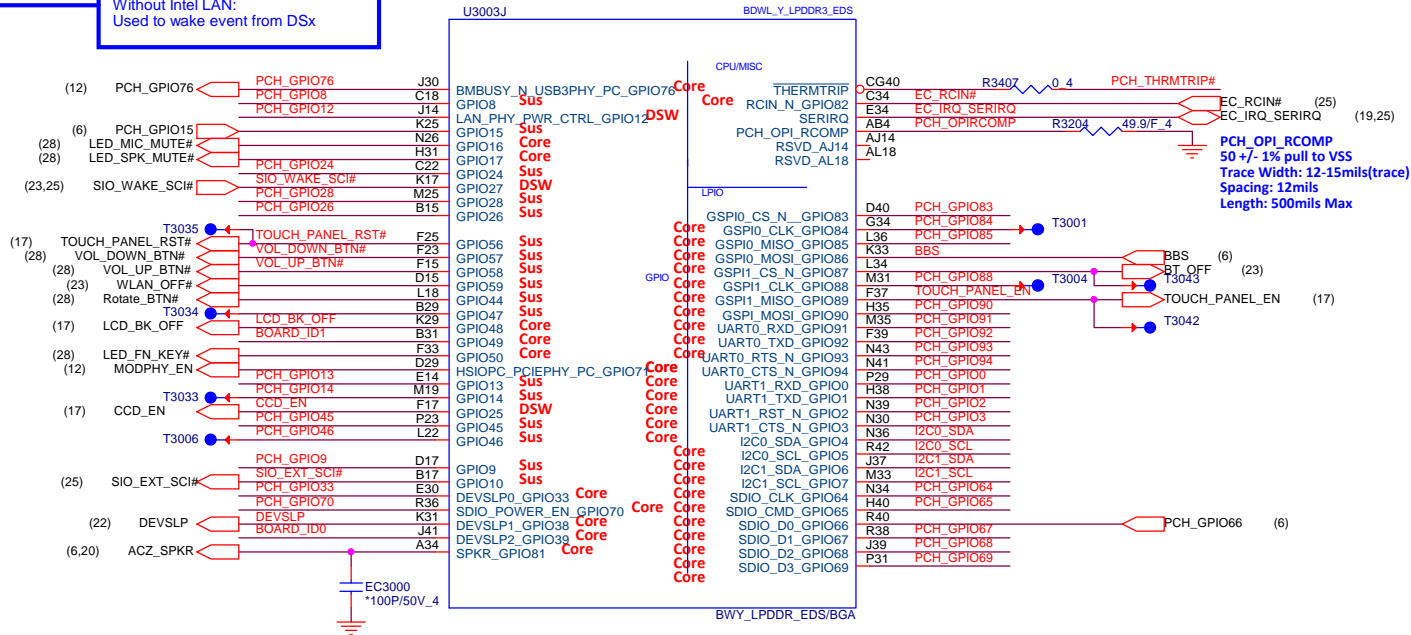
SKU	PCH_GPIO55	PCH_GPIO54	PCH_GPIO53	PCH_GPIO52
4Gb_Micron_A die *4PCS	0	0	0	0
4Gb_Micron_A die *8PCS	0	0	0	1
4Gb_Samsung_D35Q *4PCS	0	0	1	0
4Gb_Samsung_D35Q *8PCS	0	0	1	1
4Gb_Hynix_A die *4PCS	0	1	0	0
4Gb_Hynix_A die *8PCS	0	1	0	1



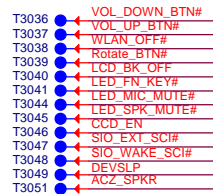
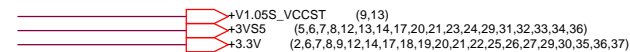
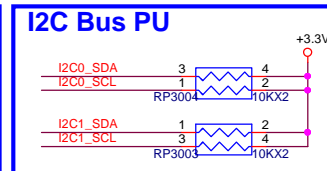
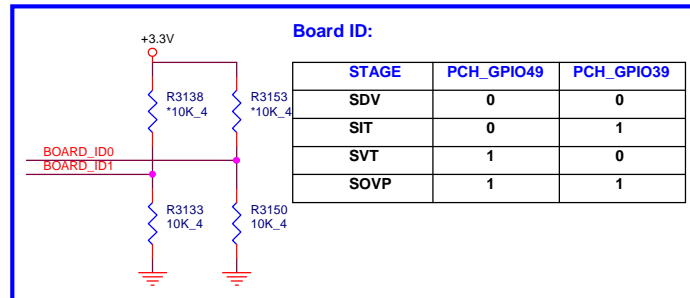
## Broadwell Type-Y ULT(GPIO,LPIO,MISC)

## GPIO27

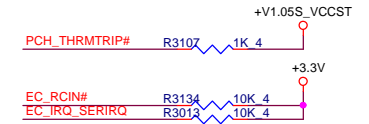
With Intel LAN:  
Connect to LANWAKE# pin on the LAN  
Without Intel LAN:  
Used to wake event from DSx



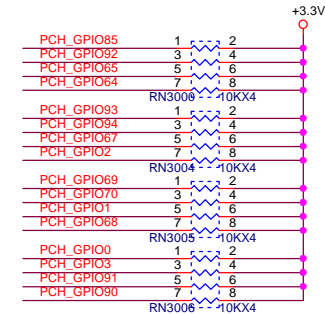
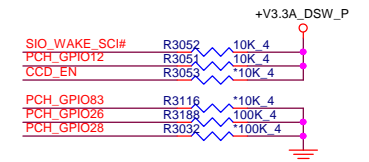
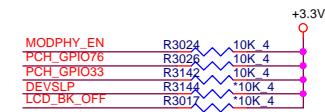
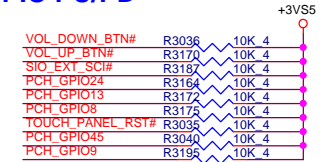
Note:  
 GSPI,UART,I2C and SDIO are only supported on  
 the system that enable Connected Standby



## CPU MISC PU/PD



## GPIO PU/PD

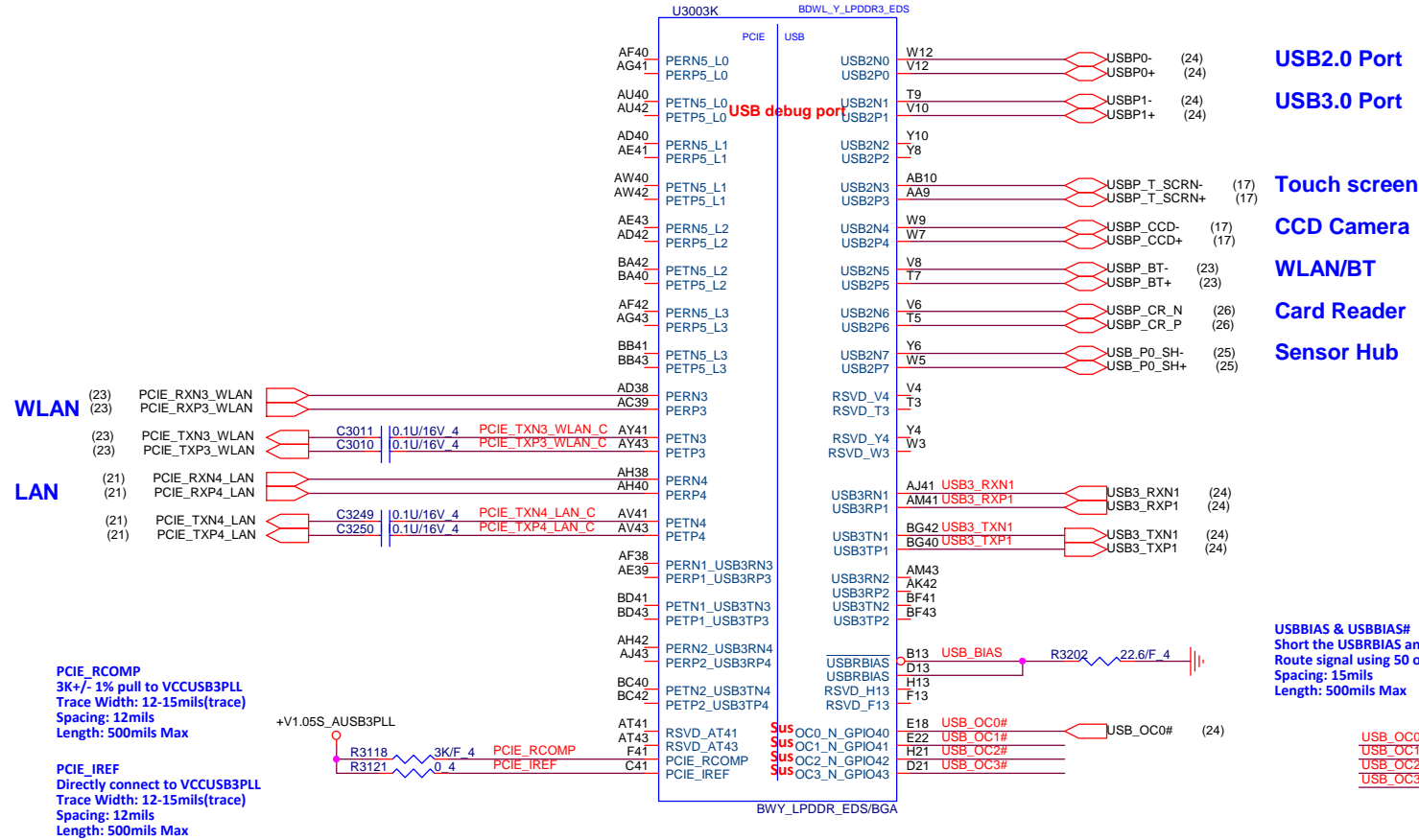


PROJECT : LI6  
Quanta Computer Inc.

Size	Document Number	Rev
	<b>BDW PCH(GPIO/LPIO/MISC)</b>	<b>1A</b>
Date:	Tuesday, August 19, 2014	Sheet 4 of 41

# Broadwell Type-Y ULT (PCIE,USB)

05

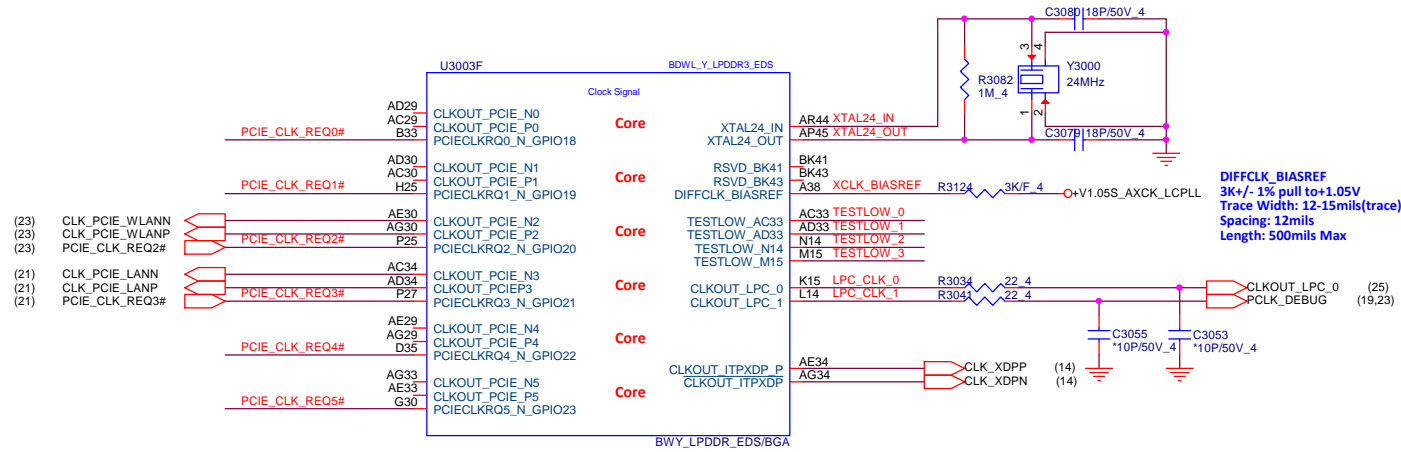




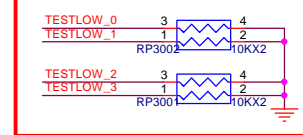
## Broadwell Type-Y ULT (CLK)

WLAN

LAN



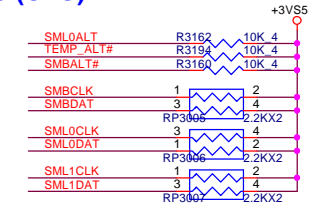
Do not short the testlow pins together.



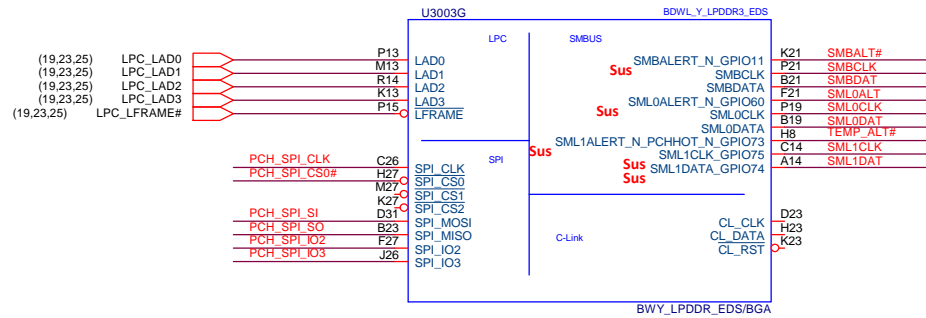
## CLK REQ PU (CLG)



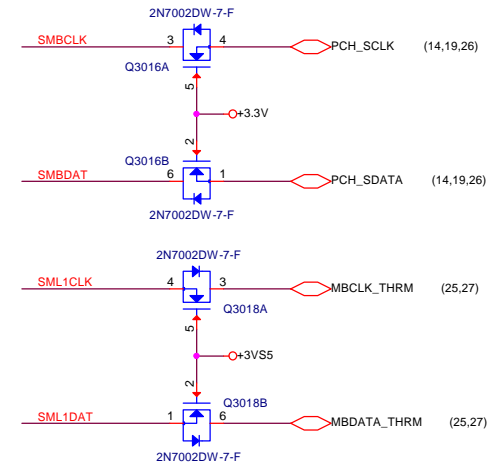
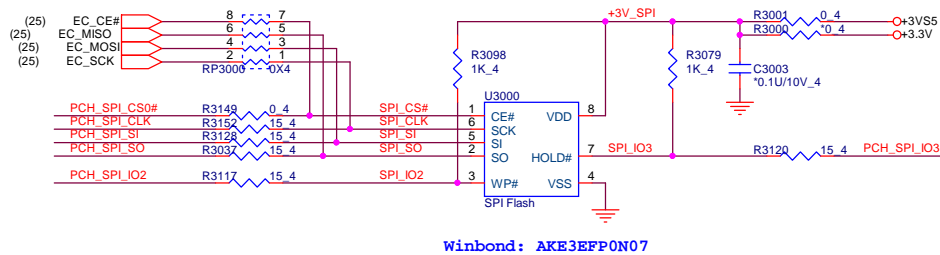
## SMBus PU (CLG)



## Broadwell Type-Y ULT (LPC/SPI/SMB/CLINK)



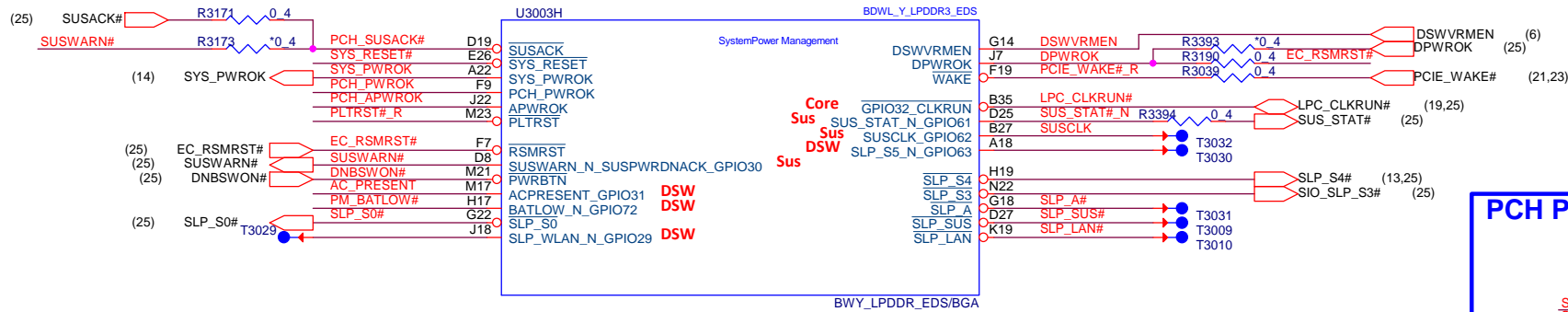
## SPI ROM for EC &amp; BIOS



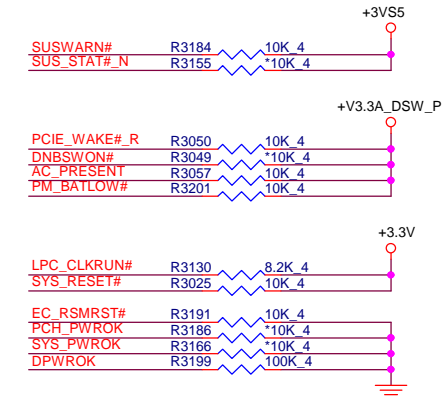
+3.3V (2,4,6,8,9,12,14,17,18,19,20,21,22,25,26,27,29,30,35,36,37)  
+3VS5 (4,5,6,8,12,13,14,17,20,21,23,24,29,31,32,33,34,36)



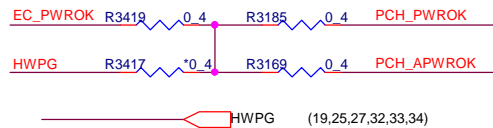
## Broadwell Type-Y ULT (SYSTEM POWER MANAGEMENT)



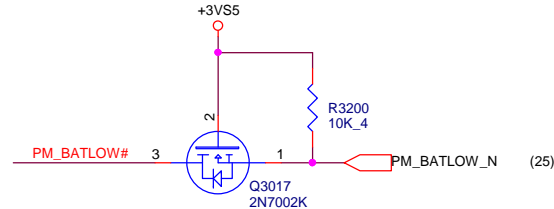
**PCH PU/PD (CLG)**



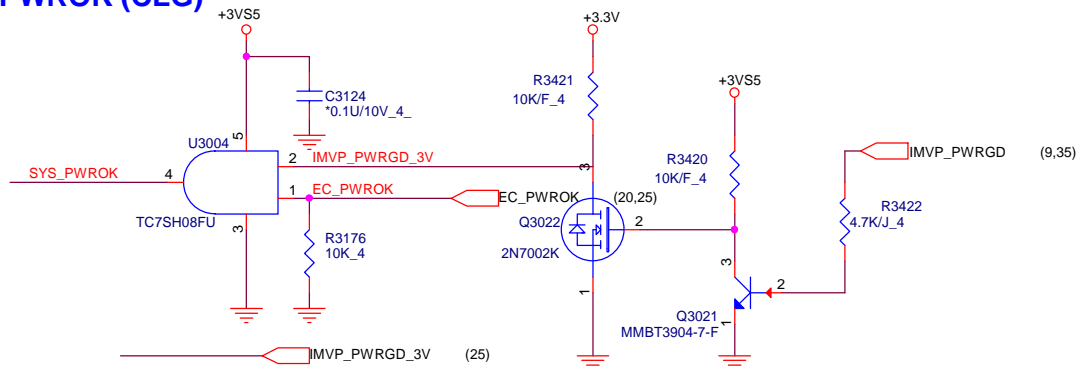
## PCH PWROK (CLG)



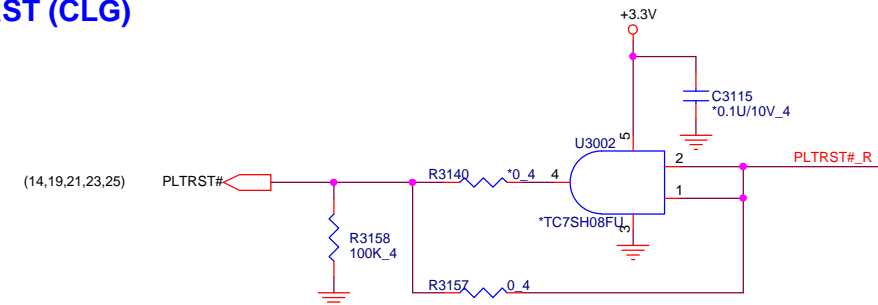
## BATLOW (CLG)



## SYS PWROK (CLG)



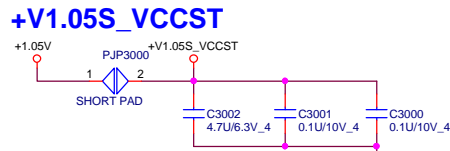
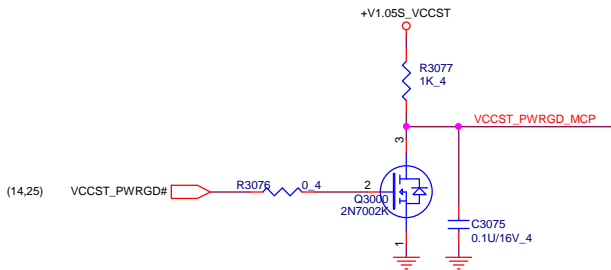
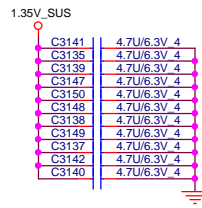
## PLTRST (CLG)





# Broadwell Type-Y ULT MCP (POWER)

09



Need to short rework after build

**SVID Bus** ALERT must be routed between CLK and DAT

**SVID CLK**

VR\_SVID\_CLK (35)

**SVID ALERT**

CPU\_SVID\_ALERT# (35)

**SVID DATA**

VR\_SVID\_DATA (35)

VDDQ DDR3L (1.4A)

VCCST\_PWRGD\_MCP (14)

VCCST (0.1A)

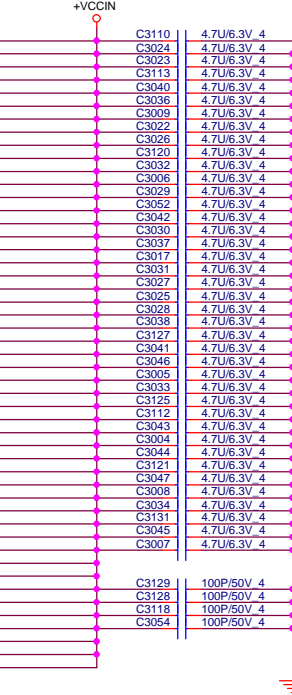
VCCST\_PWRGD\_MCP (14)

VCCST\_PWRGD\_MCP (14)

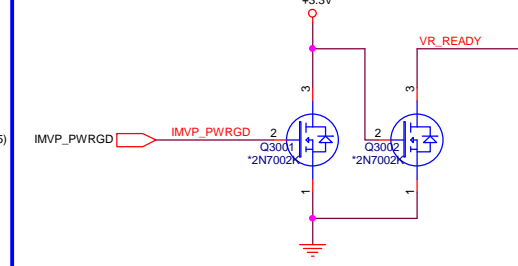
**VCCIO\_OUT OPTIONS**

VCCIO\_OUT (35)

VCC ULT 15W (32A)



**VR\_READY LS 3/3**

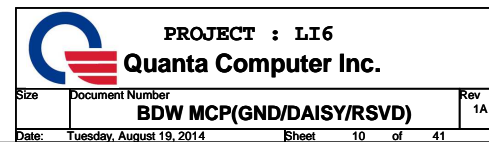


VCCIN (35)



PROJECT : LI6  
Quanta Computer Inc.

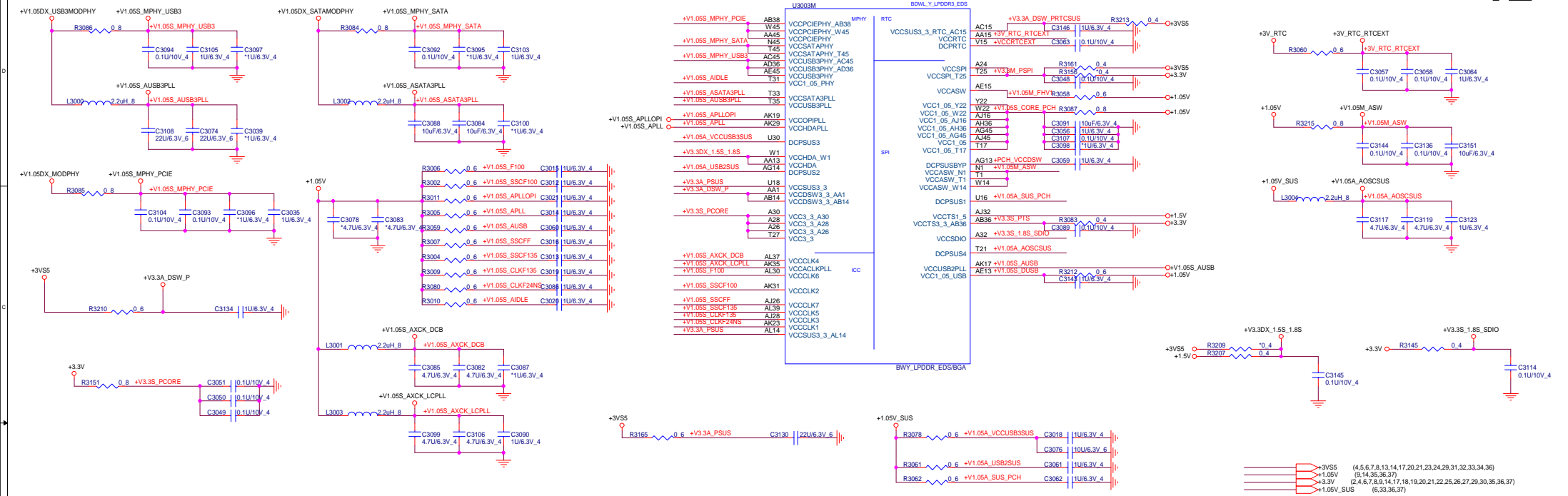
Size Document Number  
BDW MCP(POWER)  
Date: Tuesday, August 19, 2014 Sheet 9 of 41 Rev 1A



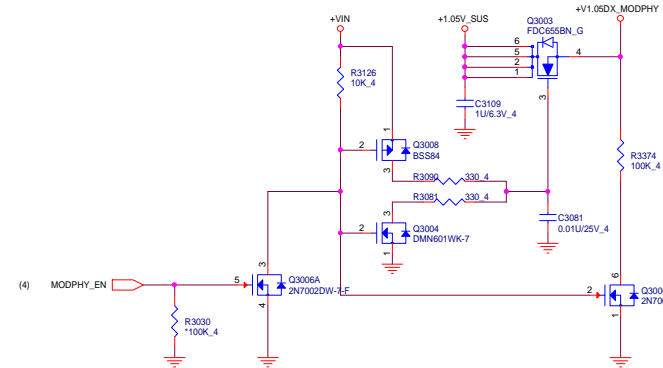


	1	0	
<b>CFG3 MSR Privacy Bit Feature</b>	Debug capability is determined by IA32_Debug_Interface_MSR (C80h) bit[0] setting	IA32_Debug_Interface_MSR (C80h) bit[0] default setting overridden	
<b>CFG4 eDP Enable</b>	DISABLED	ENABLED	

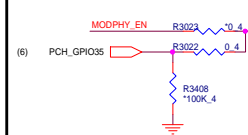
## Broadwell Type-Y ULT PCH(POWER)



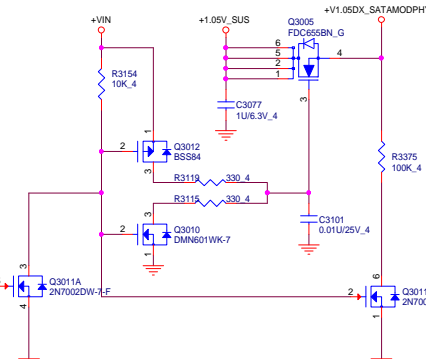
+V1.05DX\_MODPHY



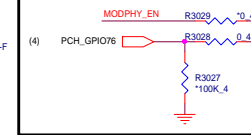
12/03 Modify



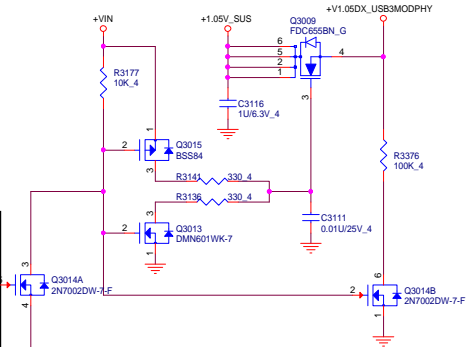
+V1.05DX\_SATAMODPHY



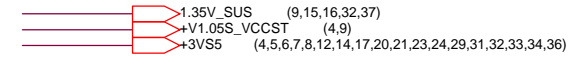
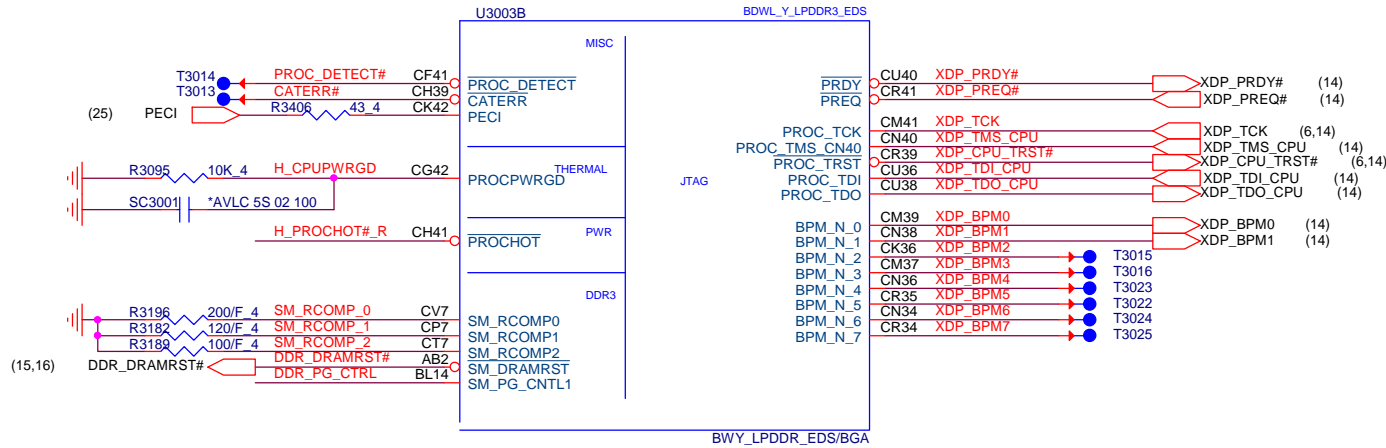
12/03 Modify



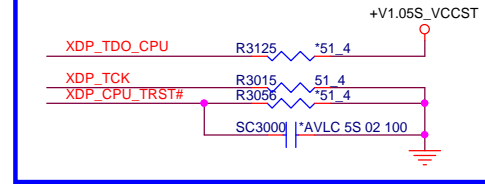
+V1.05DX\_USB3MODPHY



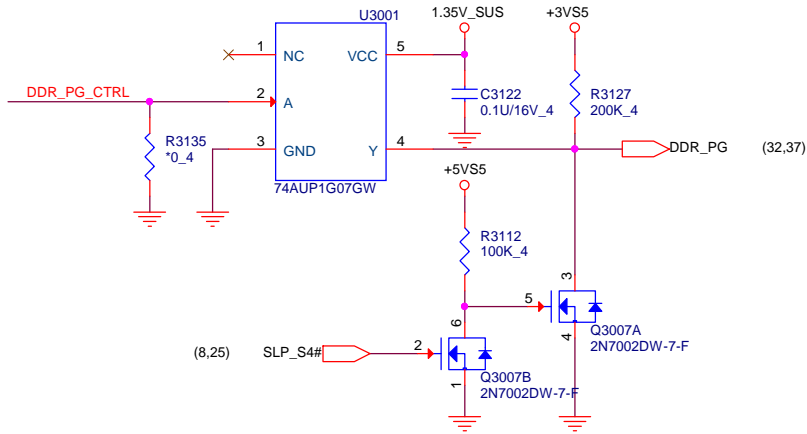
## Broadwell Type-Y ULT MCP (SIDE BAND)



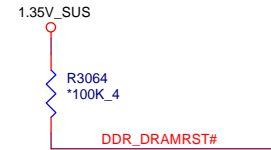
### CPU XDP PU/PD



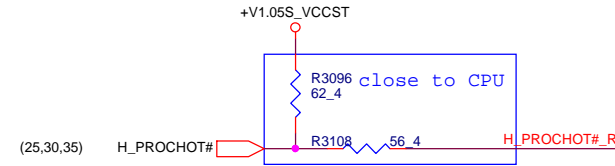
### DDR PG CNTL



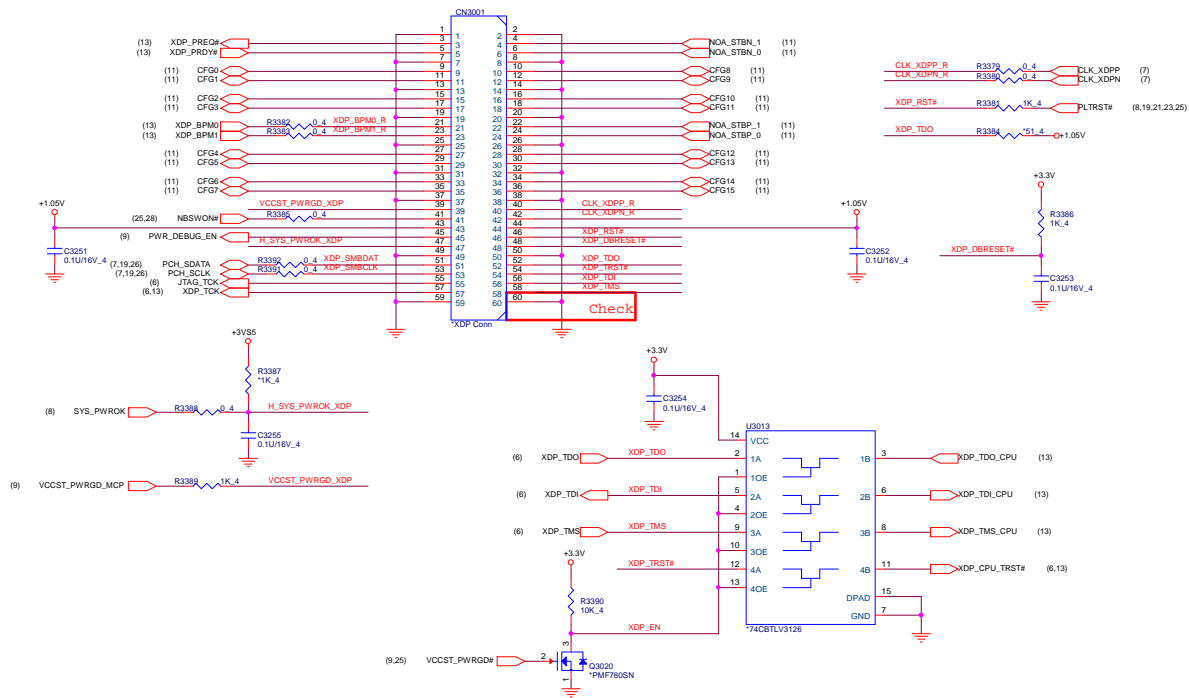
### SM\_DRAMRST#

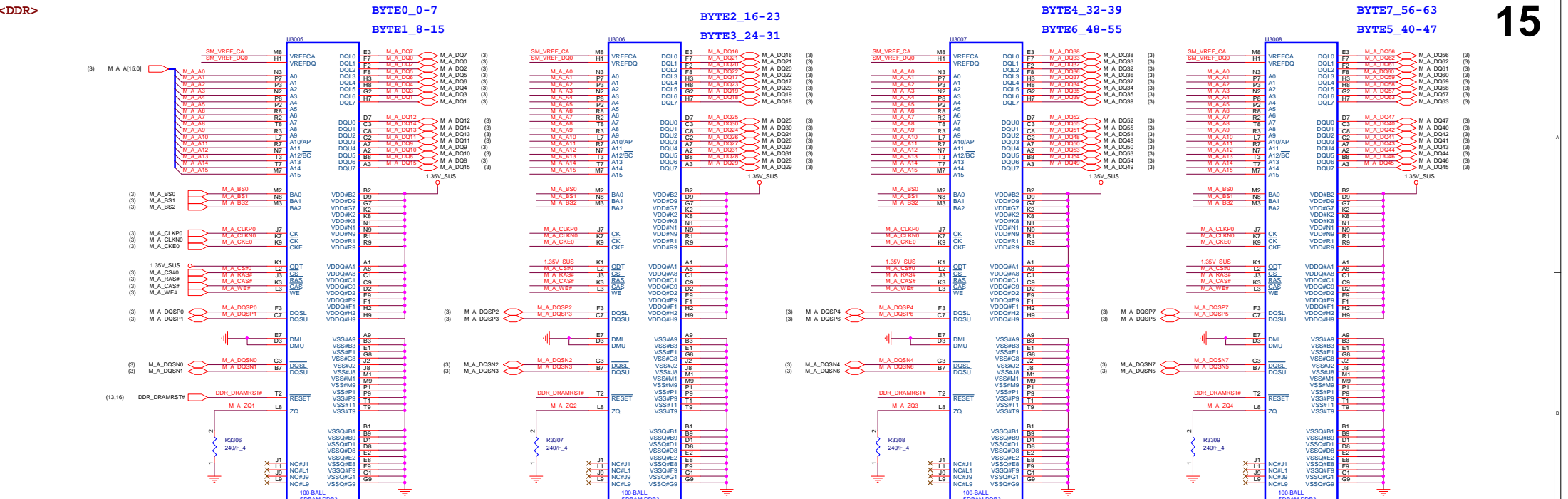


### PROCHOT#

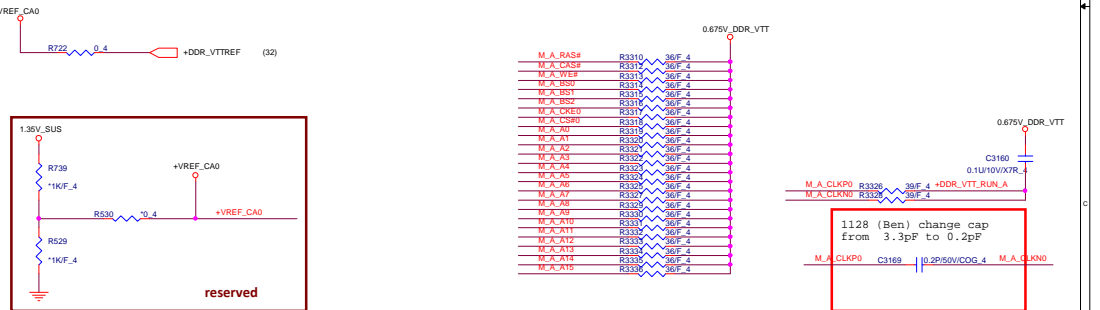
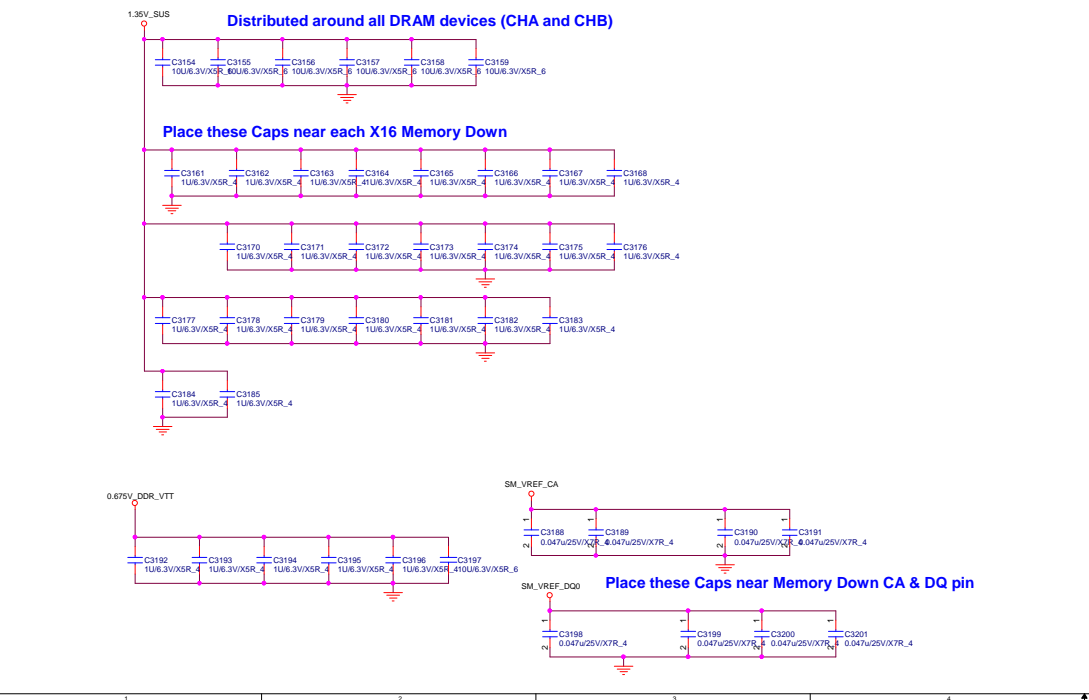


+1.05V (9,12,35,36,37)  
 +3.3V (2,4,6,7,8,9,12,17,18,19,20,21,22,25,26,27,29,30,35,36,37)  
 +VSS (4,5,6,7,8,12,13,17,20,21,23,24,29,31,32,33,34,36)





Vendor	P/N
Hynix	AKD5JGETW00-H5TC4G63AFR-PBA
Elpida	AKD5JGST400 DDR3L 1333MHz 4Gb
	AKD5JGST404 DDR3L 1600MHz 4Gb





<DDR>

BYTE2\_16-23

BYTE2\_24-31

BYTE1\_0-7

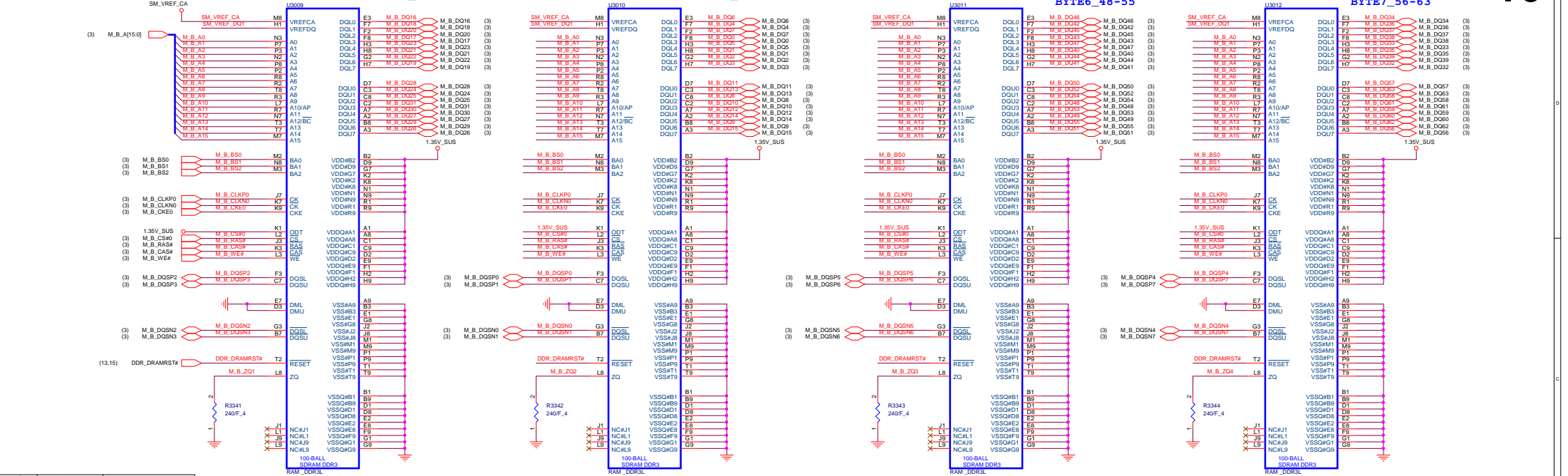
BYTE1\_8-15

BYTE5\_40-47

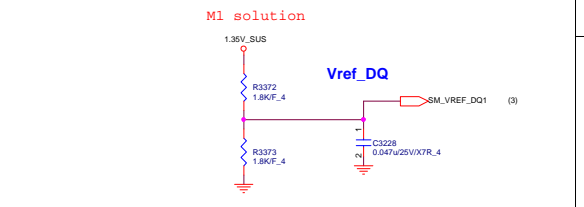
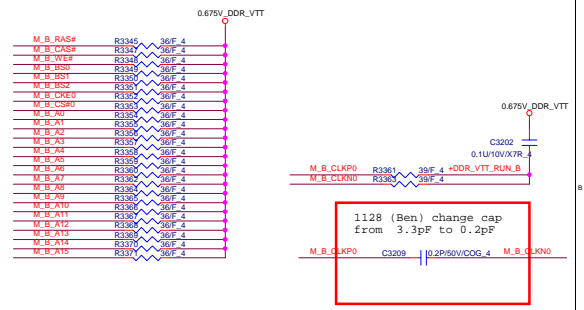
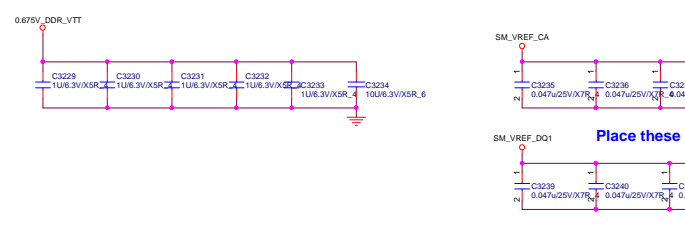
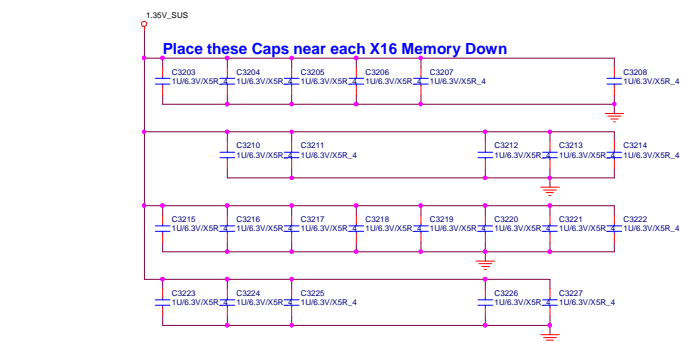
BYTE6\_48-55

BYTE4\_32-39

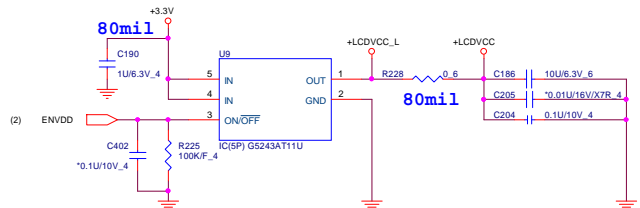
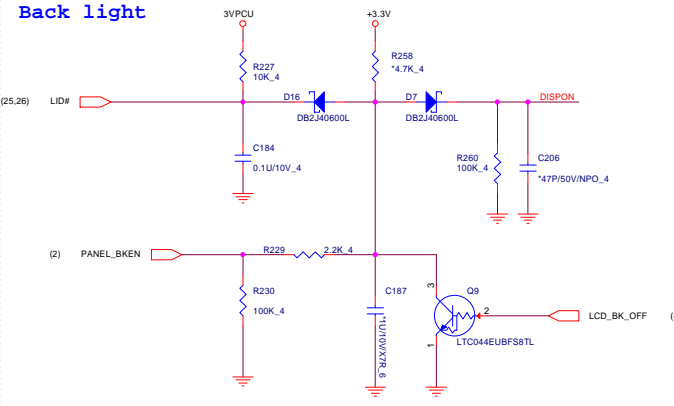
BYTE7\_56-63



Vendor	P/N
Micron	AKD53GSTL02 MT41K256M16HA-125-E
Elpida	AKD53GST400
	AKD53GST404



(2) ENVDD

[illegible]

**GFX\_PWR\_SRC**

VIN

R266 0.8

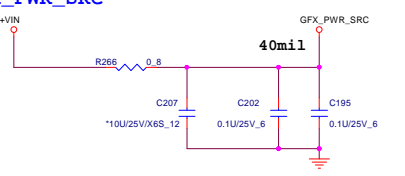
40mil

C207 10u/25V/X6S\_12

C202 0.1u/25V\_6

C195 0.1u/25V\_6

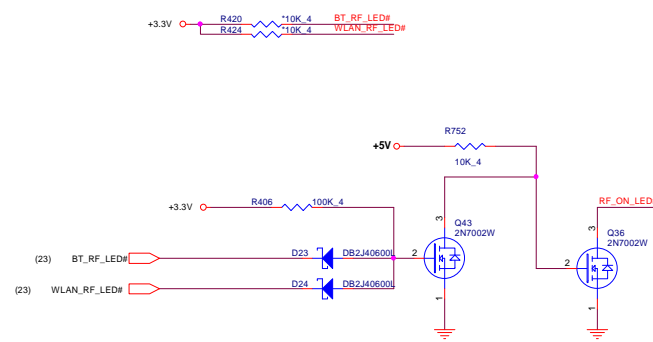
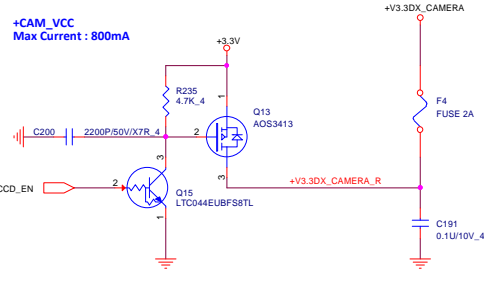
GFX\_PWR\_SRC



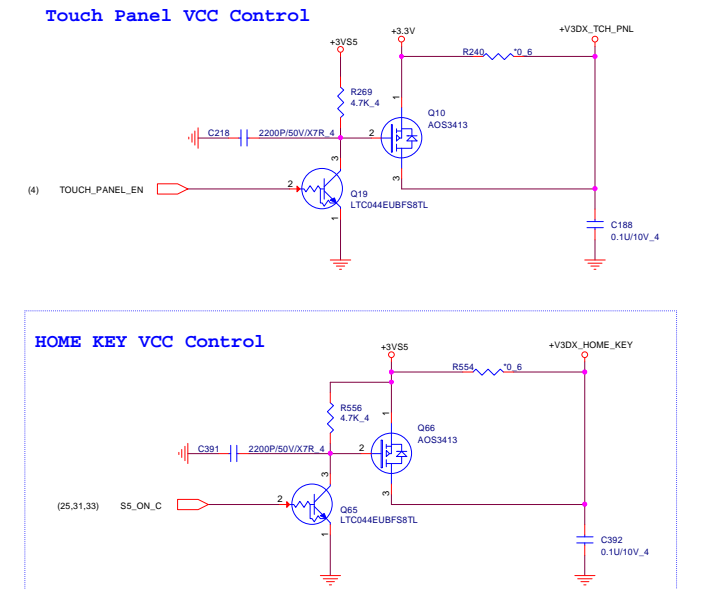
### CAMERA VCC Control

**+CAM\_VCC**  
Max Current : 800mA

The diagram illustrates the CAMERA VCC Control circuit. It features a 3.3V power source connected to a fuse (F4, 2A) and a capacitor (C191, 0.1uF/10V). The circuit includes two MOSFETs: Q13 (AOS3413) and Q15 (LTC044EUBF8TL). Q13's gate is driven by a 3.3V source, and its drain is connected to a resistor (R235, 4.7K) and another 3.3V source. Q15's gate is controlled by the CCD\_EN signal, and its drain is connected to the +V3.3DX\_CAMERA\_R line, which then leads to the +V3.3DX\_CAMERA output. A capacitor (C200, 2200P/50V/X7R\_4) is connected between the 3.3V source and the gate of Q13. The maximum current for +CAM\_VCC is specified as 800mA.

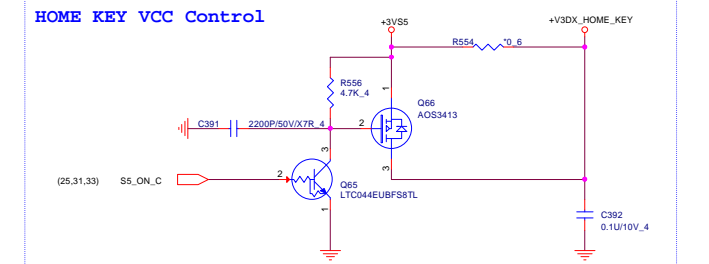
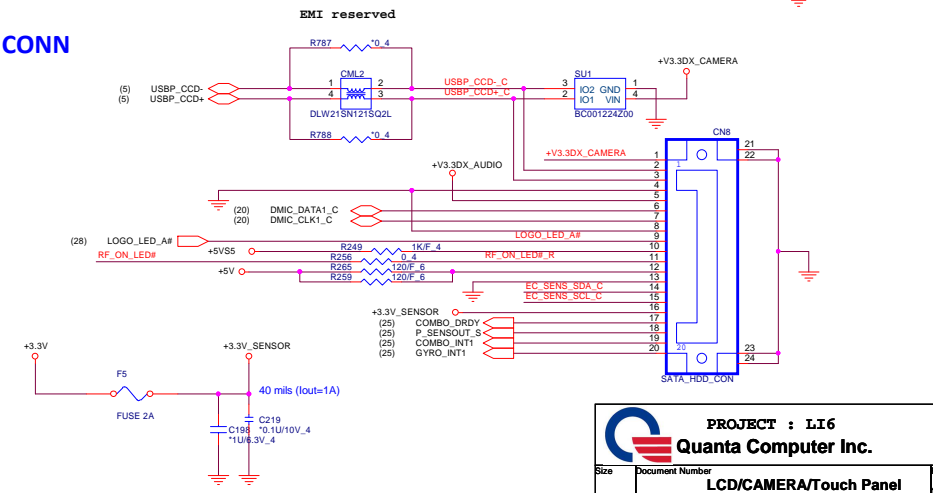


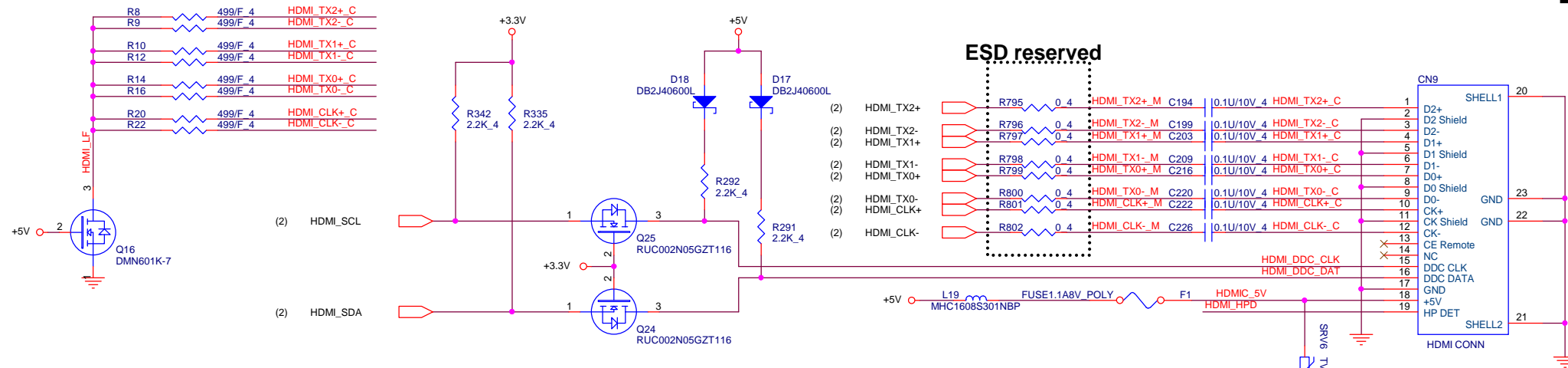
# 17



### HOME KEY VCC Control

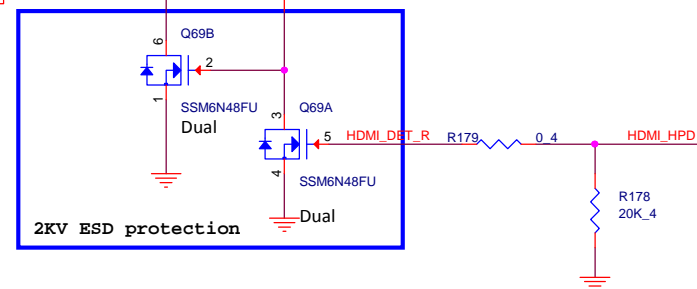
The diagram illustrates the HOME KEY VCC Control circuit. It features two MOSFETs, Q65 (LTC044EUBFS8LT) and Q66 (AOS3413). The input signal S5\_ON\_C (25.31k) is connected to the gate of Q65 through a resistor R55. The gate of Q65 is also connected to the gate of Q66. The drain of Q65 is connected to the gate of Q66. The source of Q65 is connected to ground. The drain of Q66 is connected to the +V3D5 HOME\_KEY line through a resistor R556. The source of Q66 is connected to ground. A capacitor C391 (2200pF) is connected between the gate and source of Q65. A capacitor C392 (0.1uF) is connected between the +V3D5 HOME\_KEY line and ground.

[illegible]

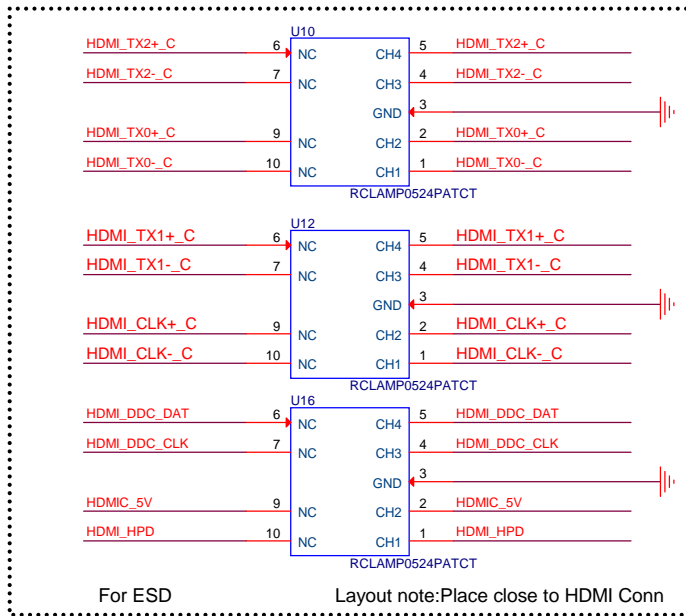
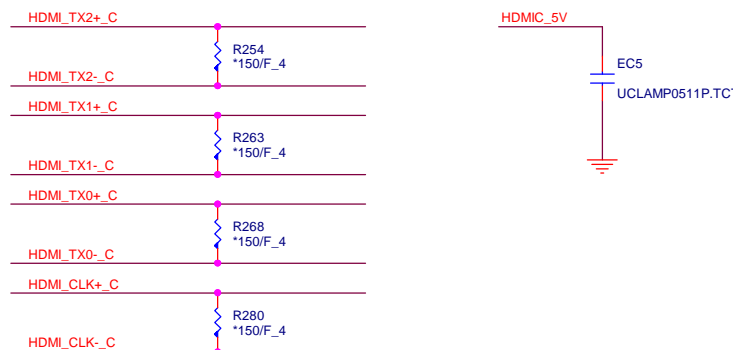


## HDMI HPD SENSE

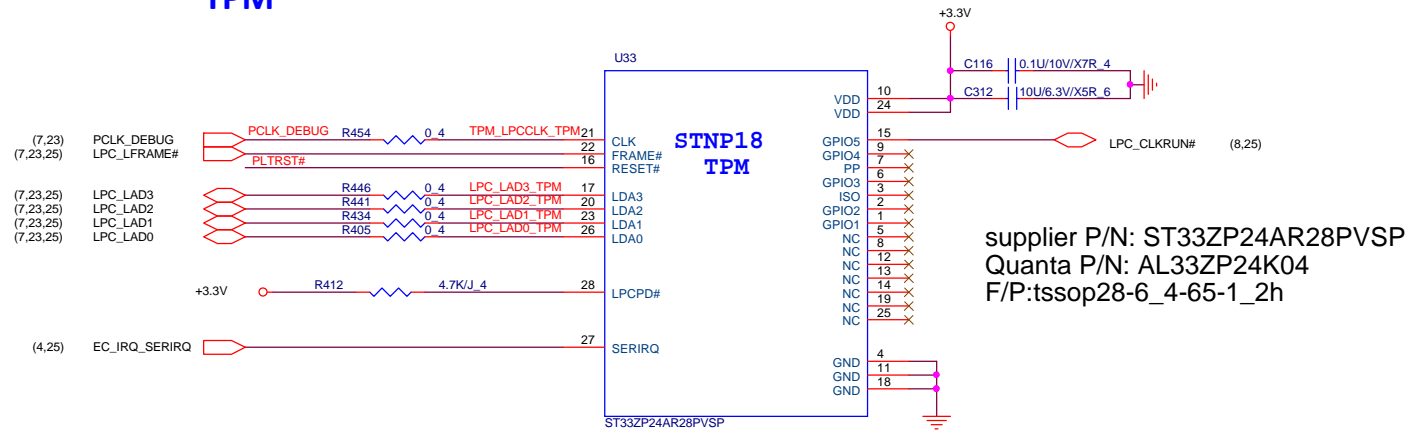
(2) HDMI\_HPQ\_Q



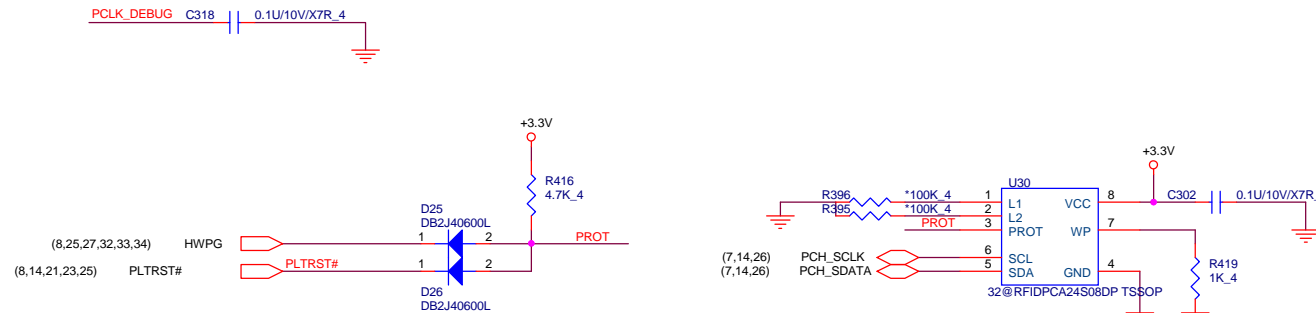
## EMI reserve for HDMI



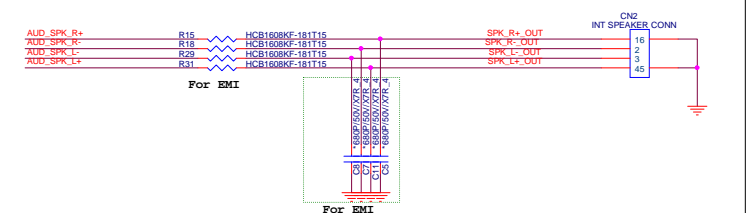
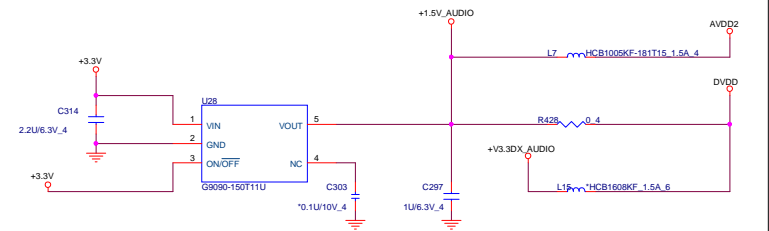
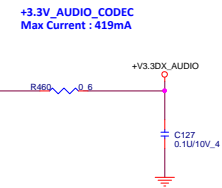
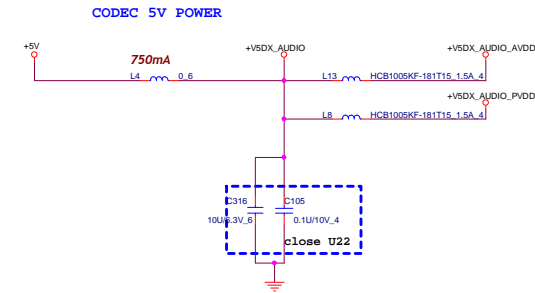
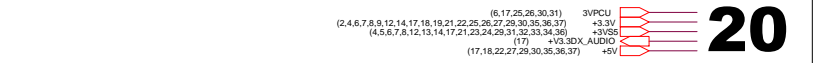
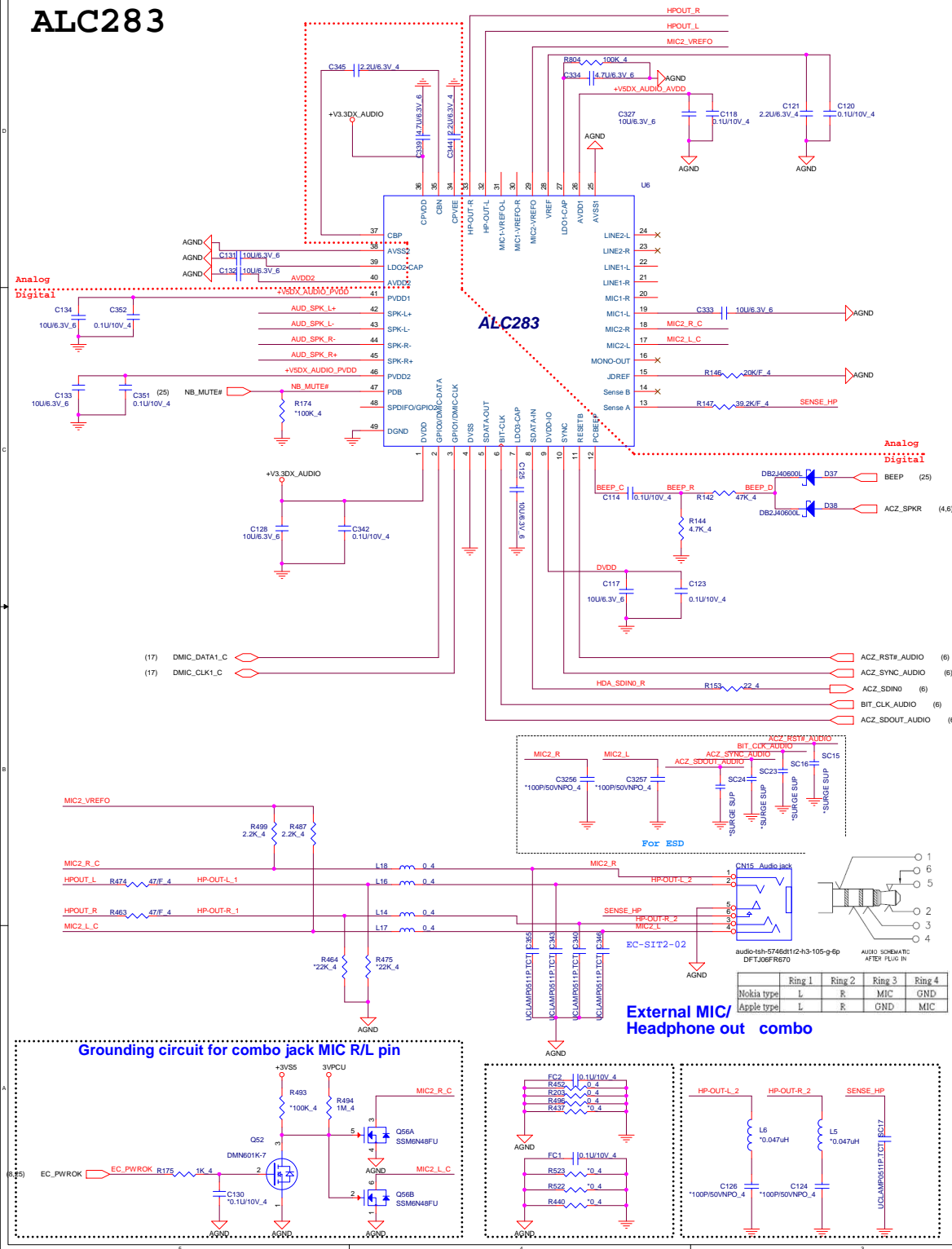
## TPM

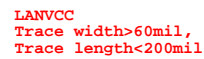


## RFID

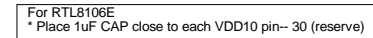


# ALC283

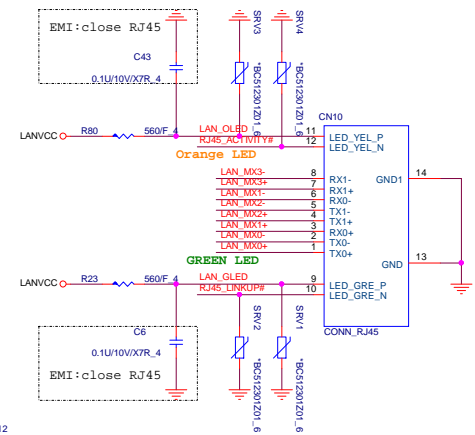


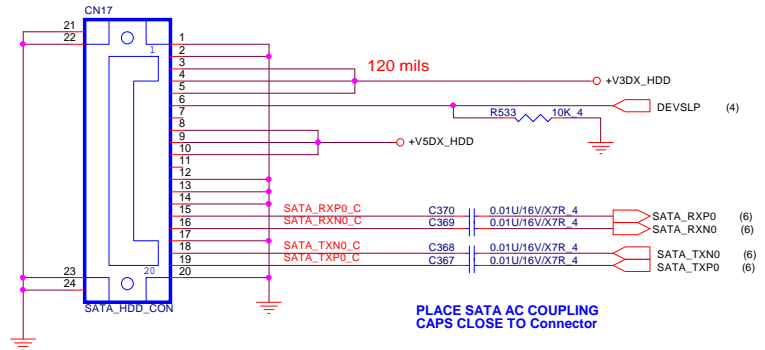


10/100	RTL8106EUS-CG	AL008106002
1G	RTL8111GUS-CG	AL008111009

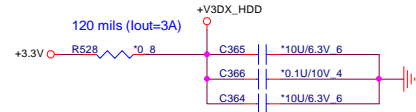


Layout: All termination  
signal should have 50 mil  
trace / 50mil spacing

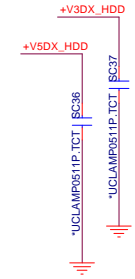
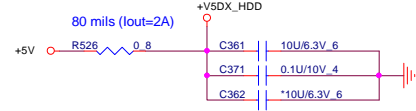




DC Current rating: 3 A (MAX)

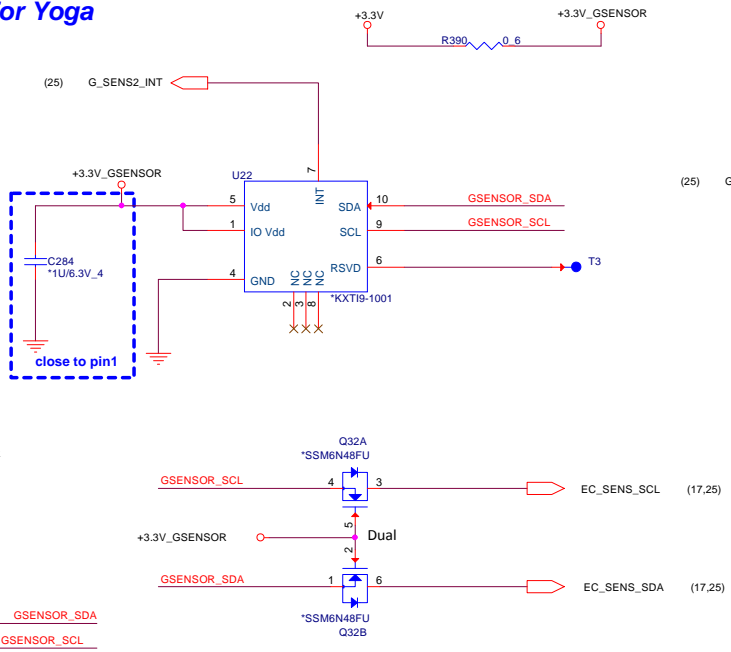


DC Current rating: 2 A (MAX)

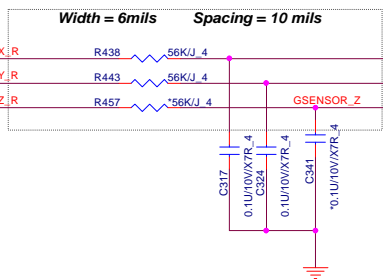
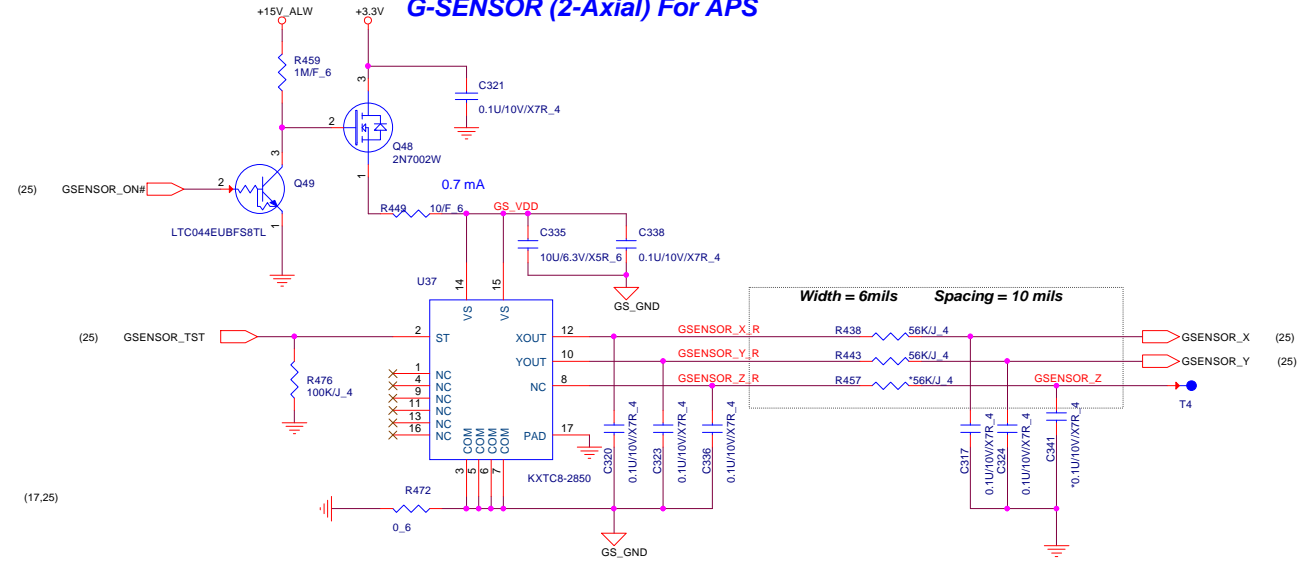


PLACE SATA AC COUPLING CAPS CLOSE TO Connector

G-SENSOR For Yoga

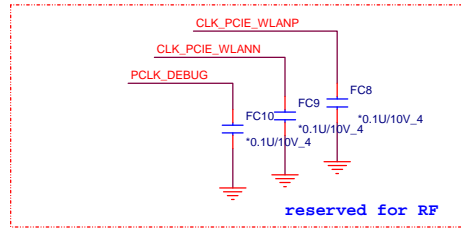
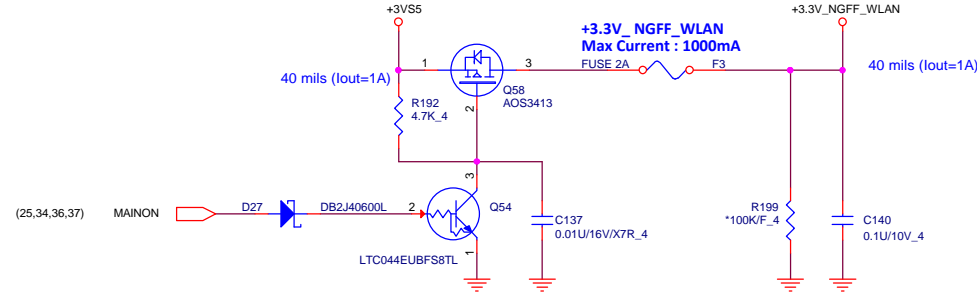
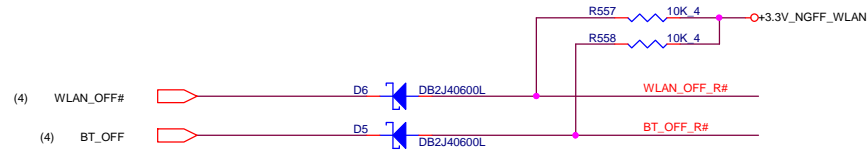
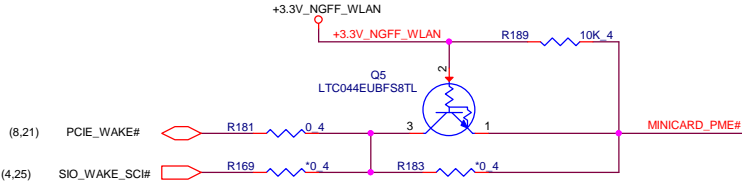
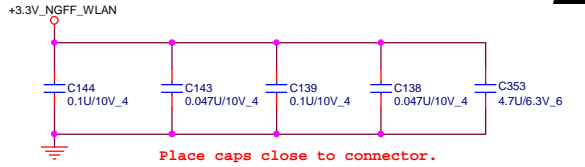
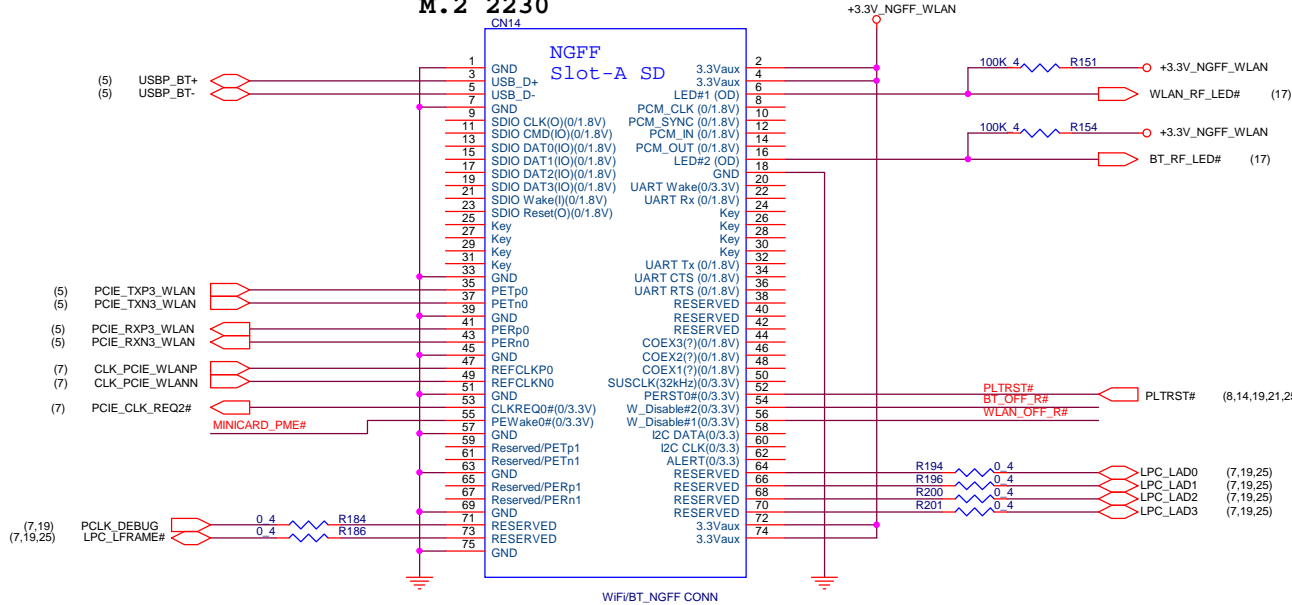


G-SENSOR (2-Axial) For APS





NGFF WiFi/BT connector  
M.2 2230



[illegible]

The schematic diagram illustrates the USB3.0 PORT1 circuit. It features three differential signal pairs: USBP1- and USBP1+ (labeled (5)), USB3\_RXN1 and USB3\_RXP1 (labeled (5)), and USB3\_TXN1 and USB3\_TXP1 (labeled (5)). Each pair is connected to a CML driver (CML1, CML7, CML8) with associated termination resistors (R783, R784, R368, R375, R381, R386) and capacitors (C278, C282). The signals are routed to a USB3.0 connector (CN12) with pins 1 (VBUS), 2 (D-), 3 (D+), 4 (GND), 5 (SSRX-), 6 (SSRX+), 7 (GND), 8 (SSTX-), 9 (SSTX+), 10 (N.C.), 13 (GND), 14 (GND), 15 (GND), and 16 (GND). The connector is labeled CONN\_USB3.0.

USB3\_RXN1

USB3\_RXP1

USB30\_TX0-\_M

USB30\_TX0+\_M

FC7

FC6

FC5

FC4

\*0.1u/10V\_4

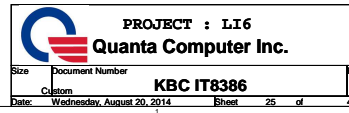
\*0.1u/10V\_4

\*0.1u/10V\_4

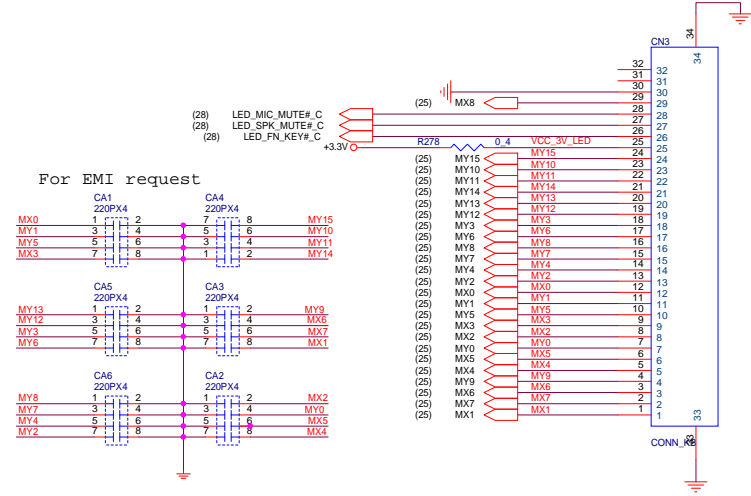
\*0.1u/10V\_4

reserved for RF

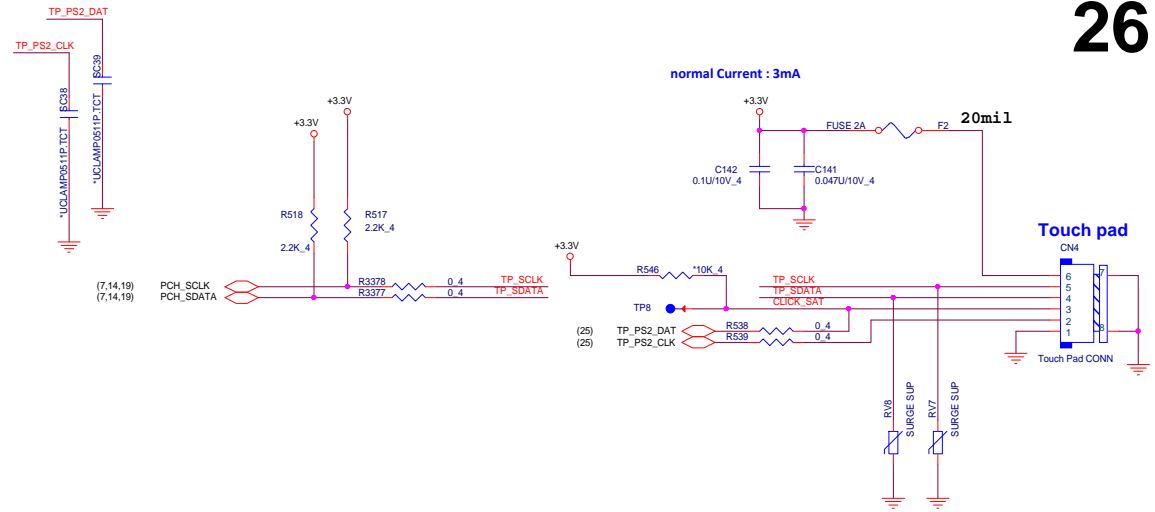
Size	Document Number	Rev
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# KEYBOARD



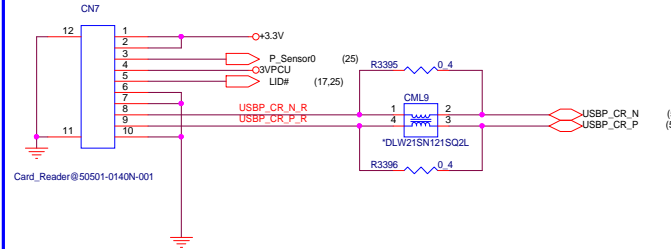
# TP Control



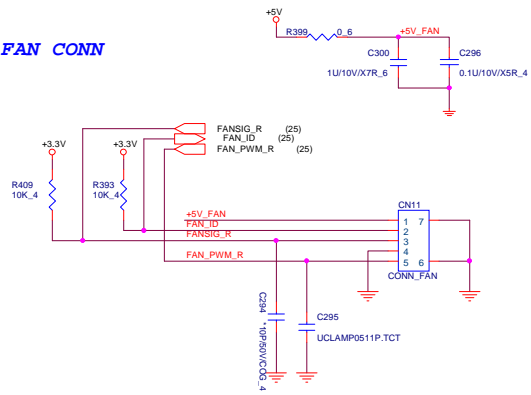
26

# Sensor/B CONN

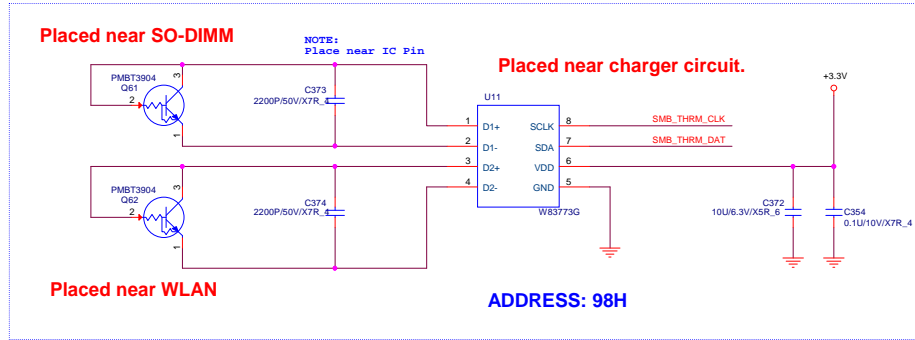
# To Card Reader Board



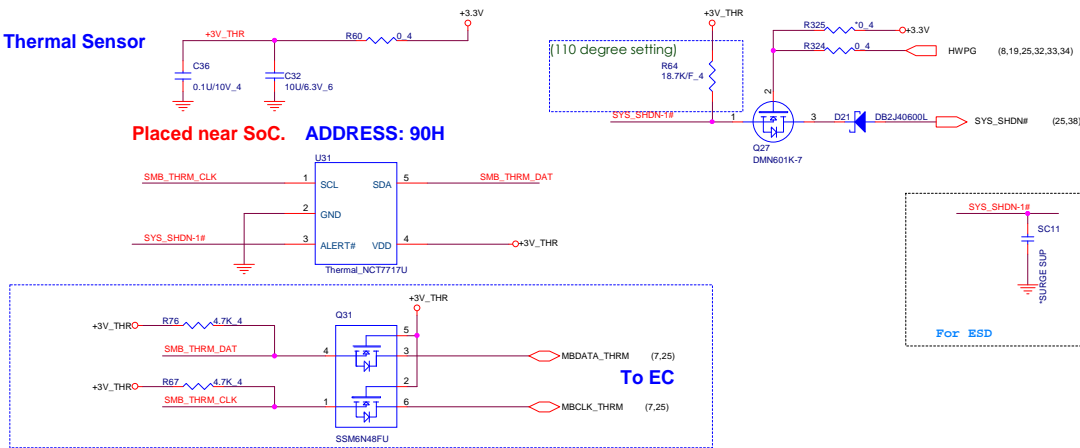
## FAN CONN



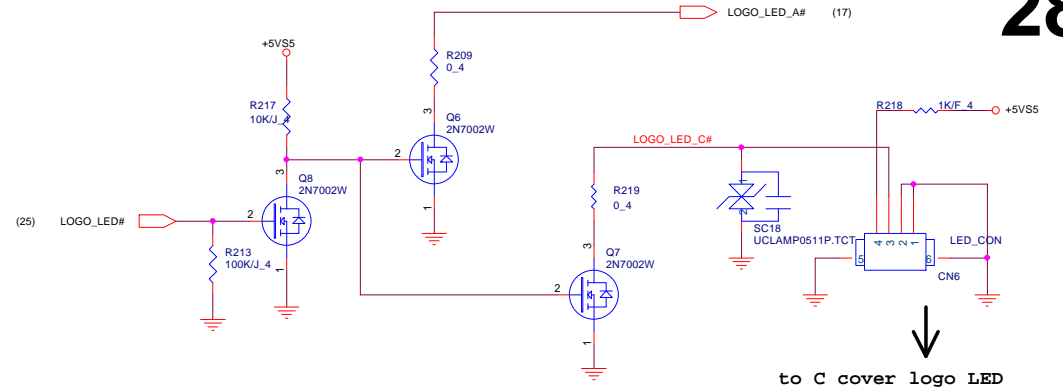
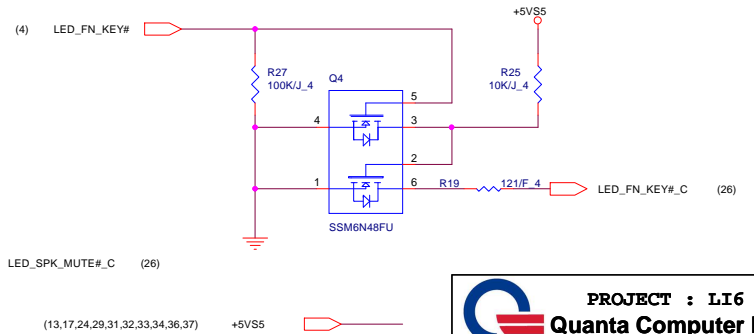
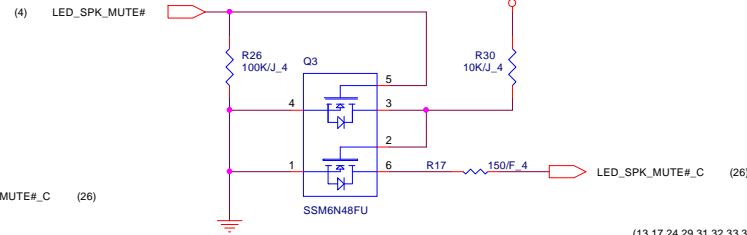
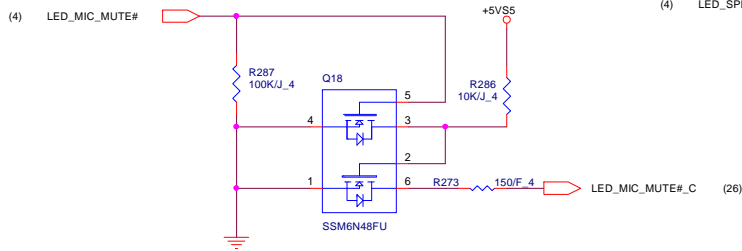
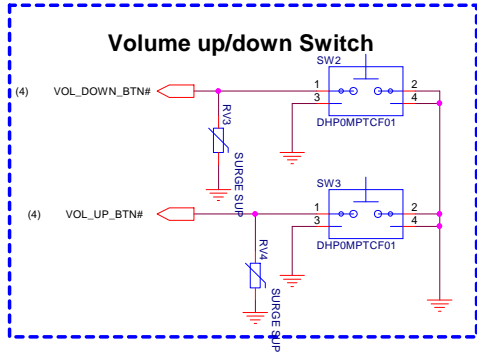
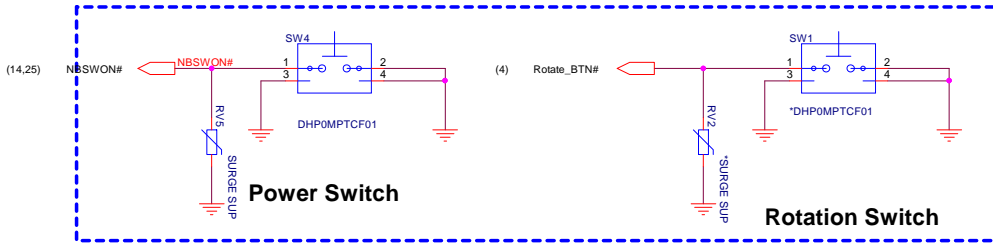
## Thermal Sensor



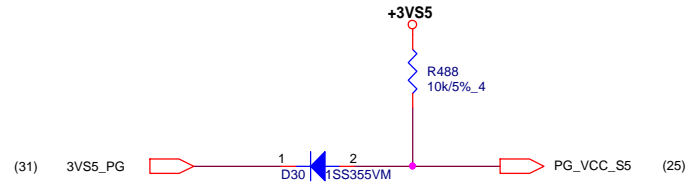
## CPU Thermal Sensor



# LED Driver

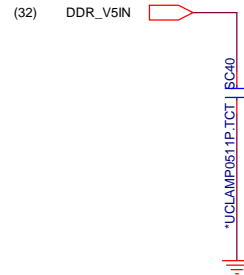
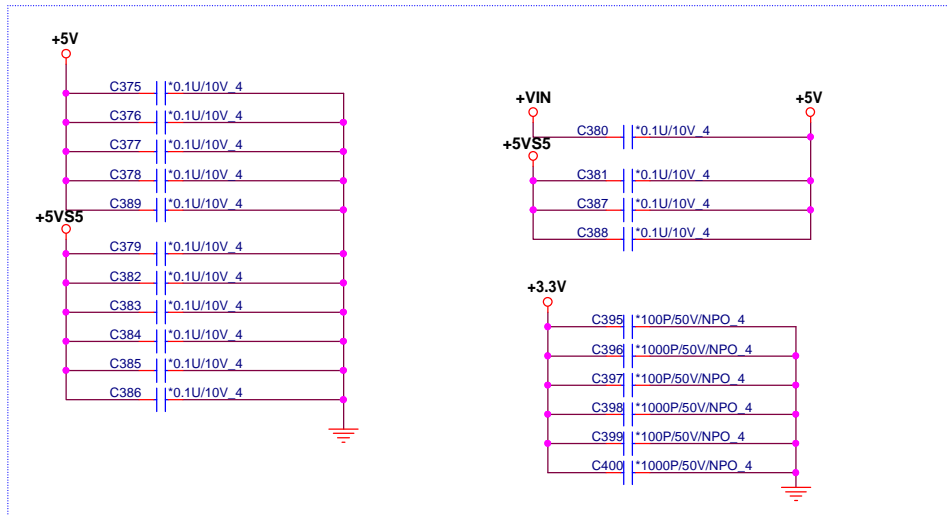
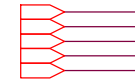


# S5 POWER GOOD

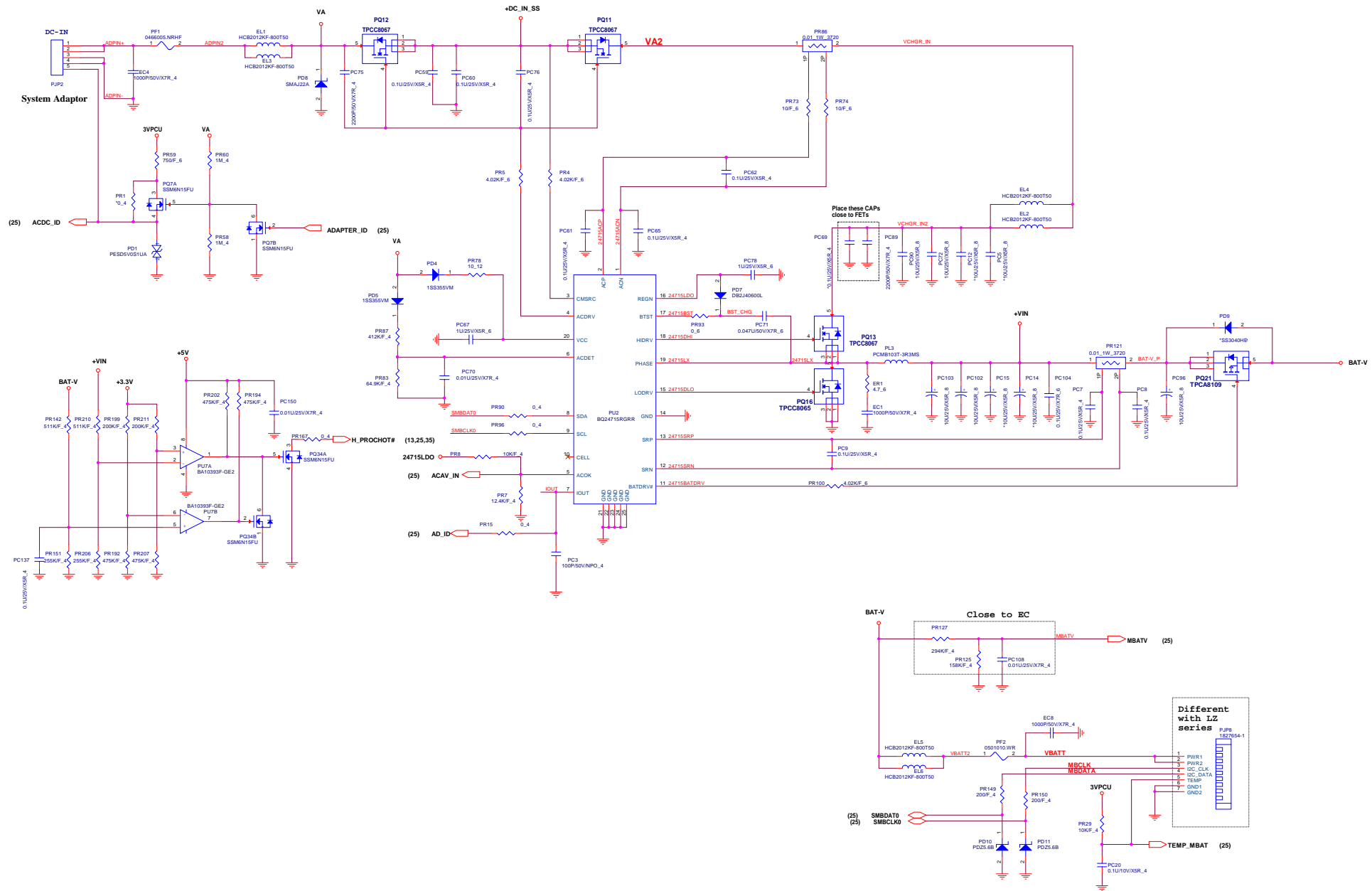


(2,4,6,7,8,9,12,14,17,18,19,20,21,22,25,26,27,30,35,36,37)  
 (4,5,6,7,8,12,13,14,17,20,21,23,24,31,32,33,34,36)  
 (17,18,20,22,27,30,35,36,37)  
 (12,17,30,31,32,33,35,38)  
 (13,17,24,28,31,32,33,34,36,37)

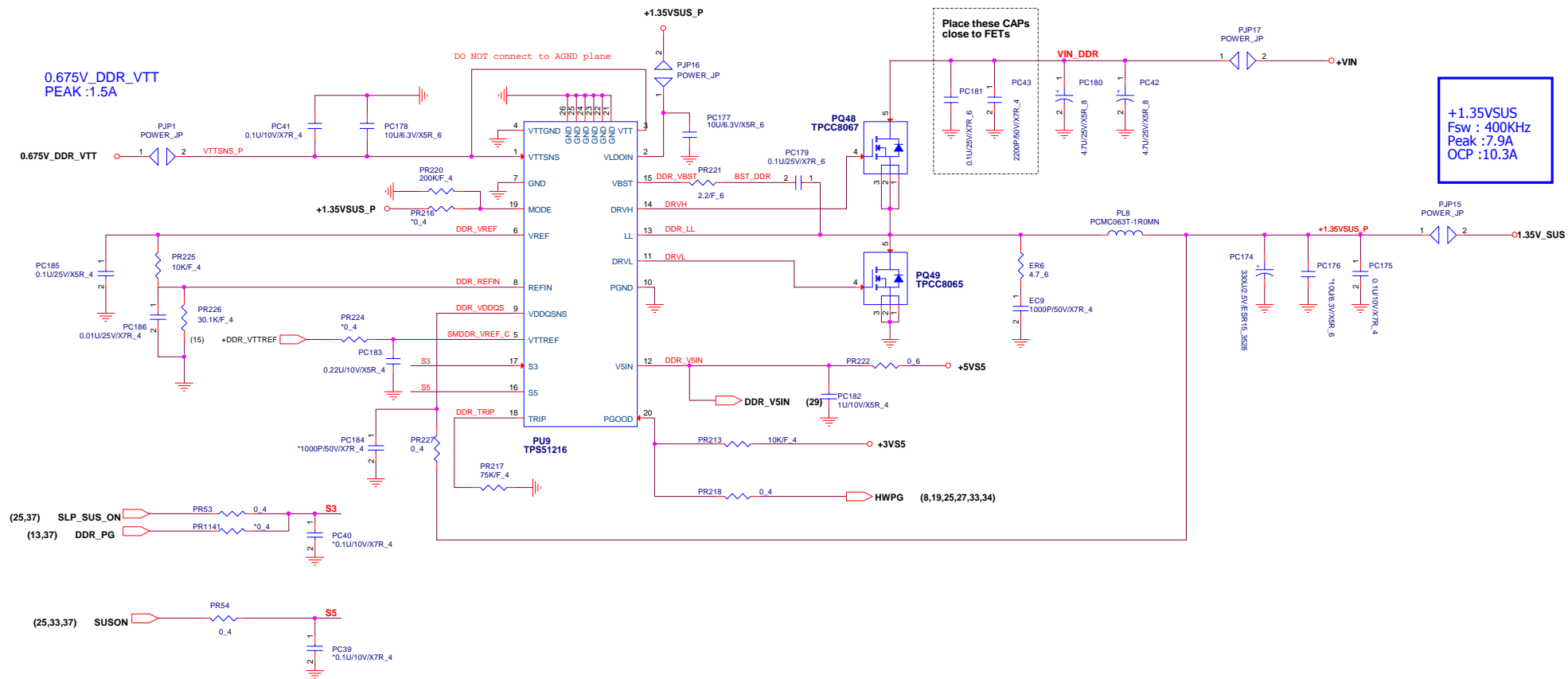
+3.3V  
 +3VS5  
 +5V  
 +VIN  
 +5VS5

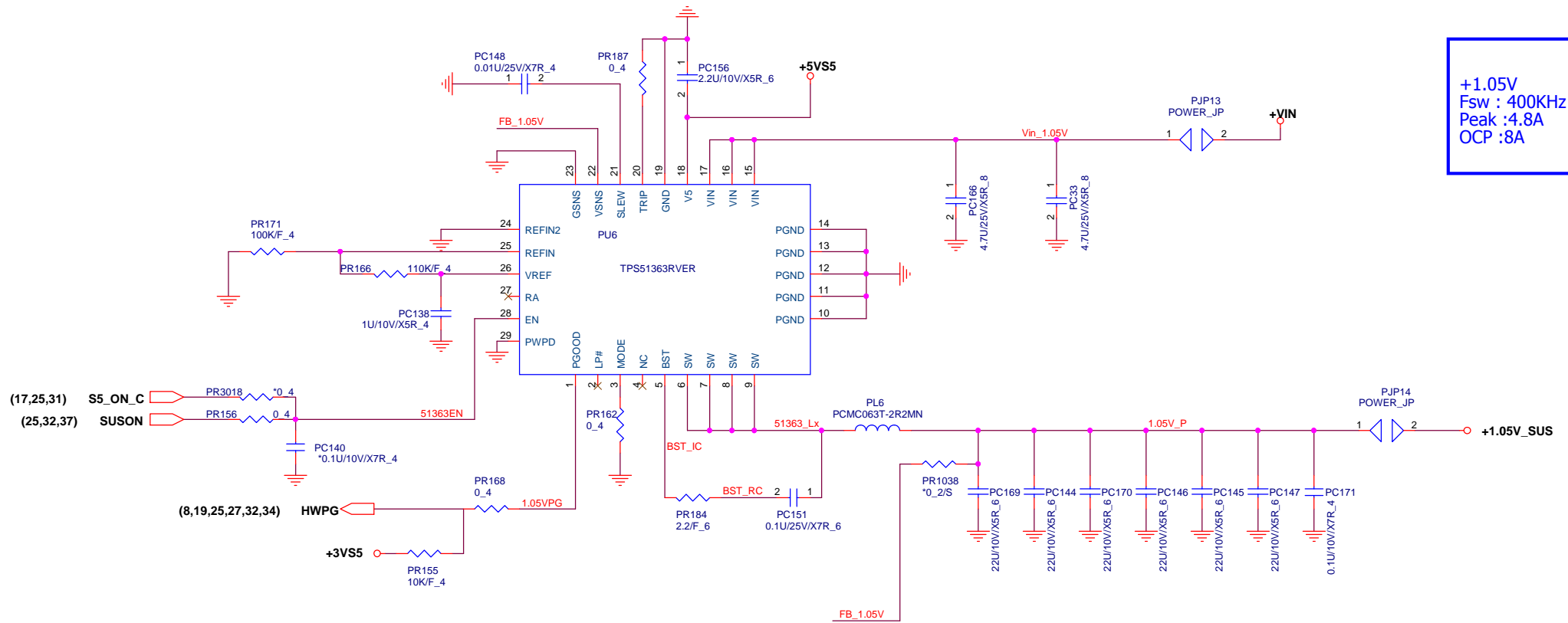




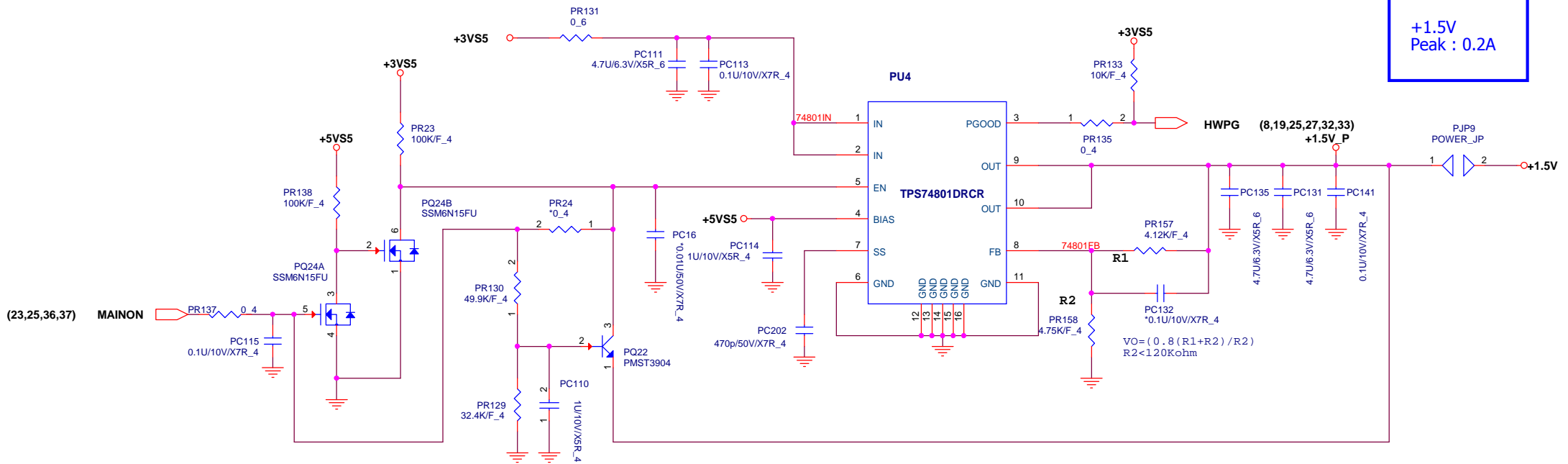





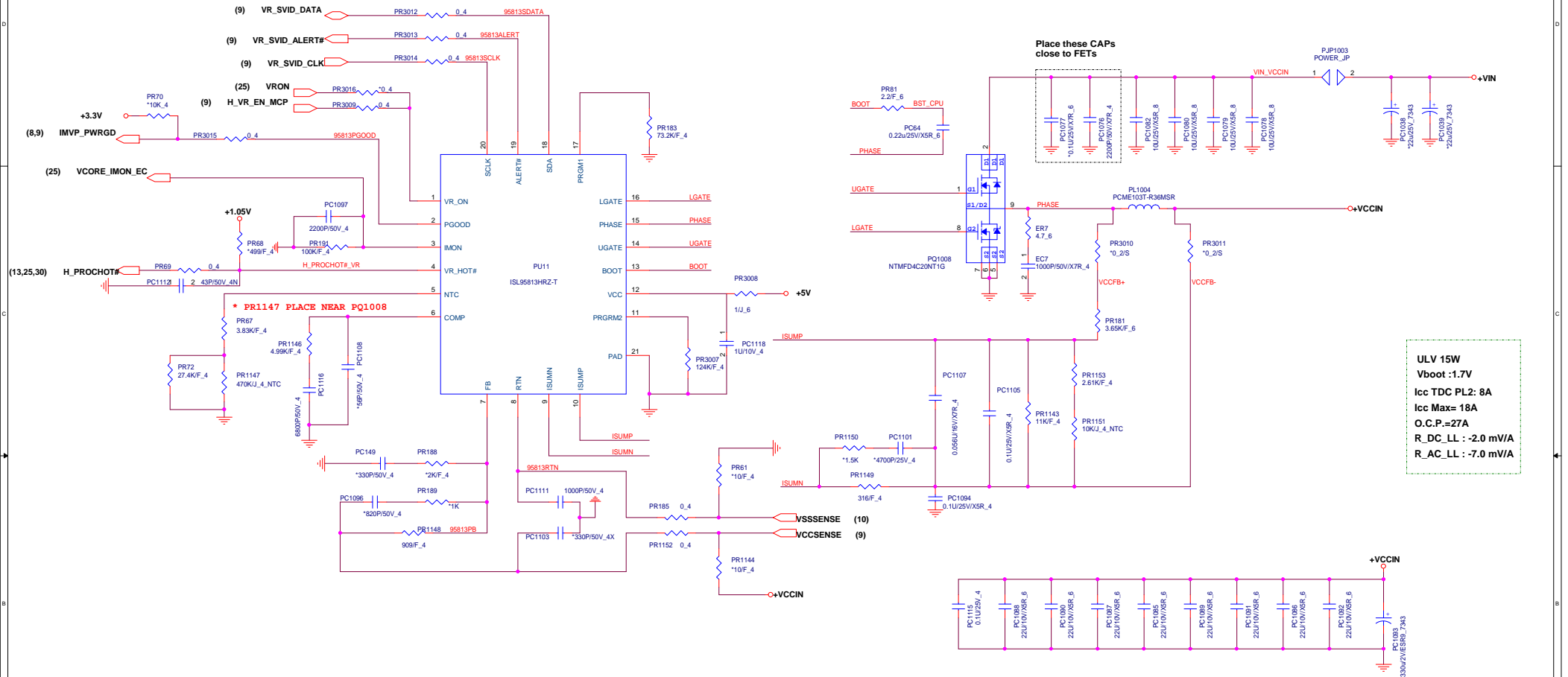




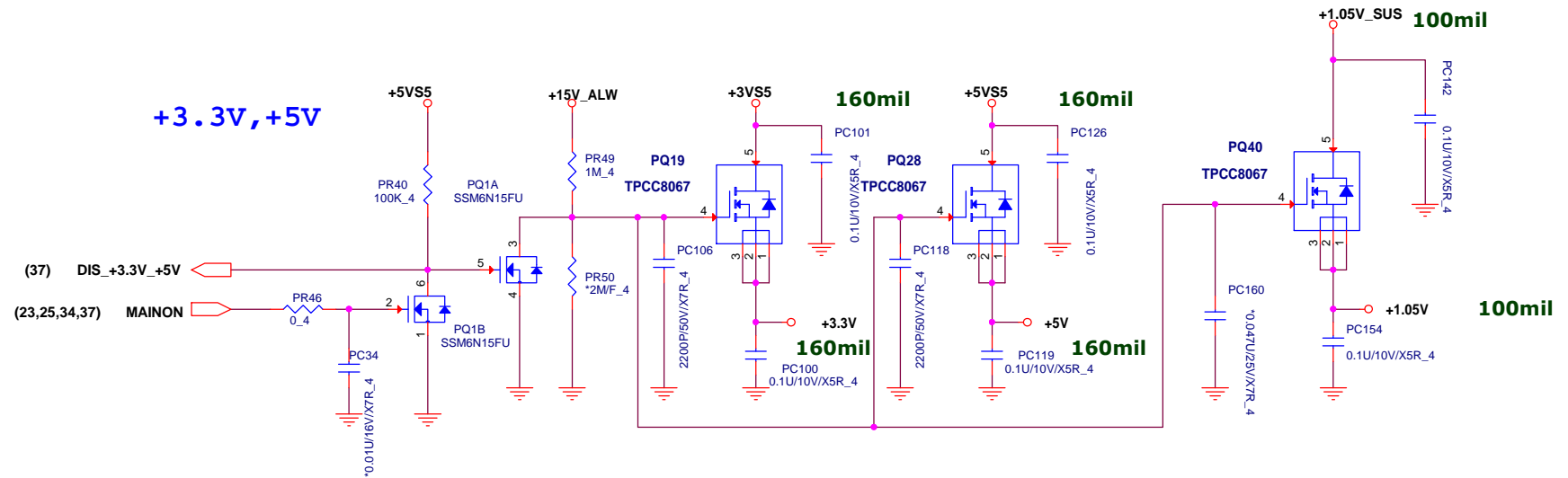
+1.05V  
Fsw : 400KHz  
Peak : 4.8A  
OCP : 8A



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	Custom		1A
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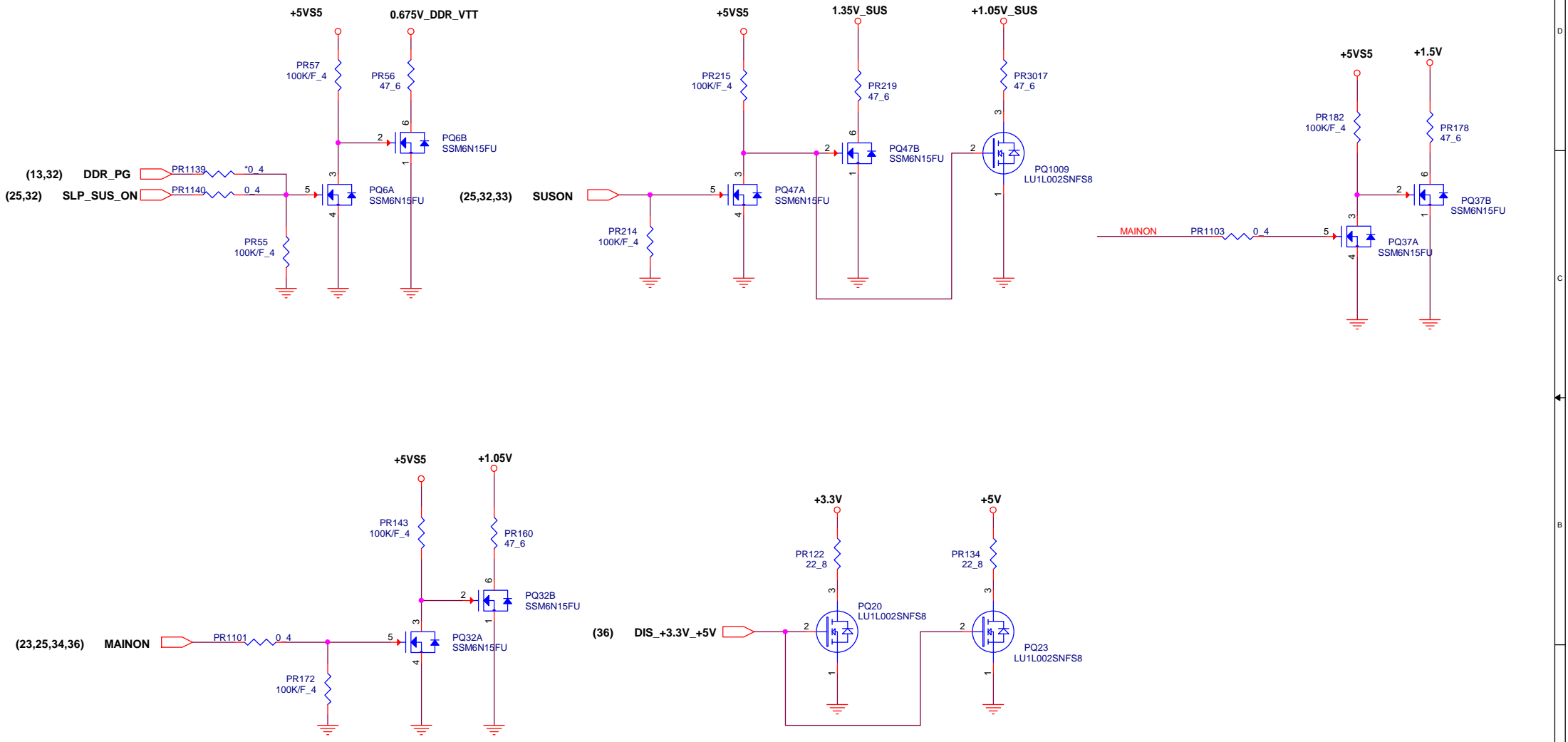


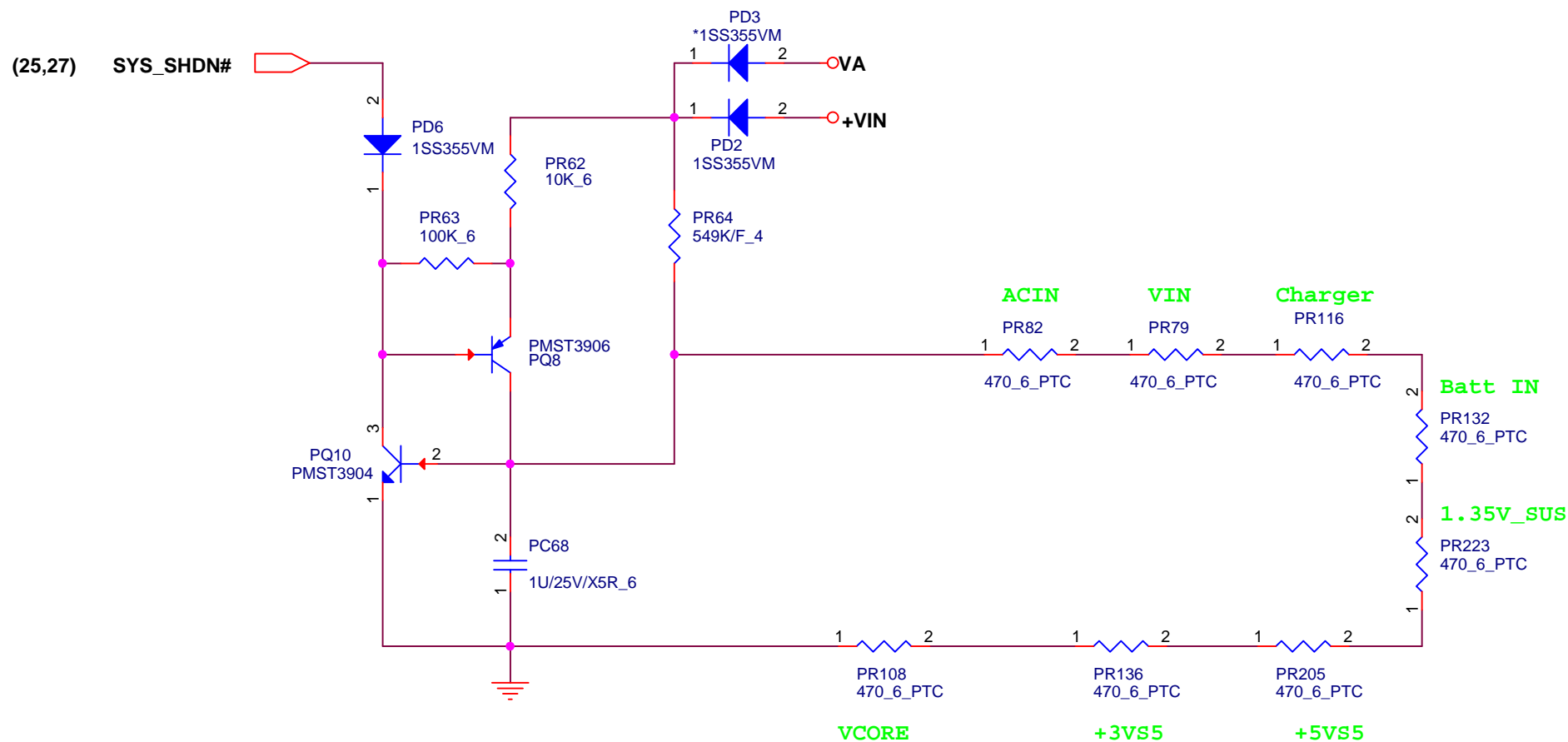
# Load switch

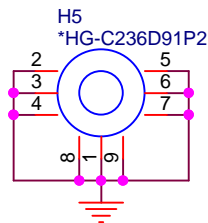
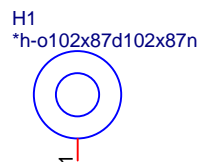
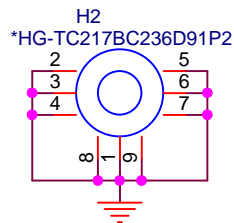
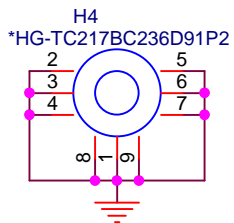
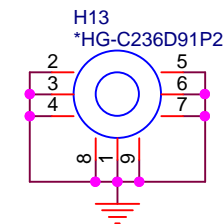
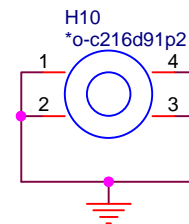
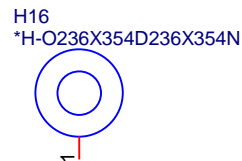
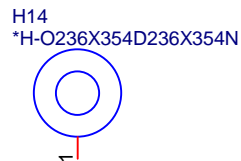
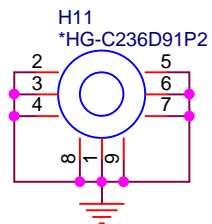
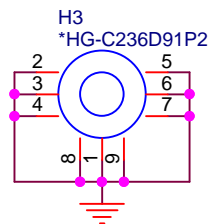




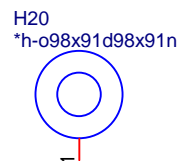
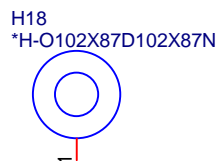
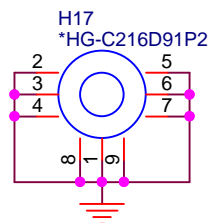
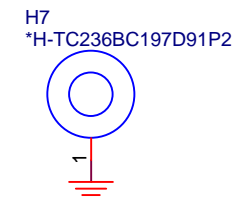
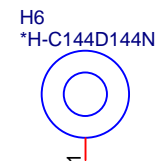
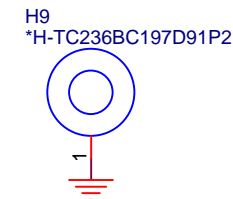
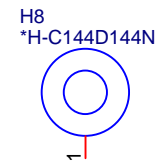
# DISCHARGE





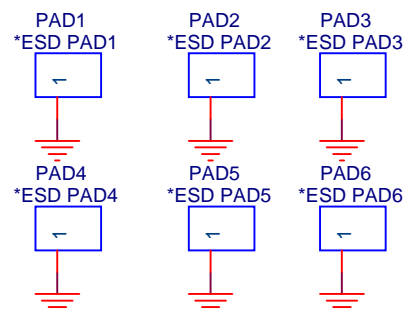
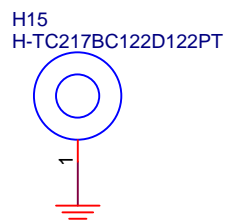


## CPU BKT Holes



## Stuff NUT Location:

### NGFF WLAN Nut



**ESD request**



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Quanta Computer Inc.

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